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1.0 SCOPE

The Board Layout and Routing Specification defines the requirements for printed circuit board (PCB) for 173359 series connector.

Disclaimer: Molex does not guarantee the performance of the final product to the information provided in this document. All information in this report is considered Molex proprietary and confidential. This guide is not intended as a substitute for engineering analysis.

Figure 1
2.1 MATERIAL THICKNESS
The pcb board material shall support required data rate. The recommended minimum pcb board thickness shall be 1.35 mm.

2.2 TOLERANCE
Maximum allowable bow of the pcb board shall be 0.08 mm over the length of the connector assembly.

2.3 HOLE DIMENSIONS
The holes for the connector cage assembly must be drilled and plated through per Figure 3.

2.4 LAYOUT
The holes for the connector assembly must be precisely located to ensure proper placement and optimum performance of the connector assembly. Recommended hole pattern, dimensions, and tolerances are provided in Figure 2A and 2B.

Recommended PC Board Layout for the Connector Assembly

[Diagram of Recommended PC Board Layout for the Connector Assembly]

Connector Figure 2A
KEEP OUT AREAS

Figure 2B

Keep out Areas
Recommended Hole Dimensions

<table>
<thead>
<tr>
<th>DIM. “A”</th>
<th>DIM. “B”</th>
<th>DIM. “C”</th>
</tr>
</thead>
<tbody>
<tr>
<td>MM / (INCH)</td>
<td>MM / (INCH) - # DRILL</td>
<td>MM / (INCH)</td>
</tr>
<tr>
<td>1.05+/-.05 (.0413+/-0.002)</td>
<td>1.181 (.0465) - # 56</td>
<td>1.40 (.055)</td>
</tr>
<tr>
<td>0.81+/-.05 (.032+/-0.002)</td>
<td>0.711 (.028) - # 70</td>
<td>1.16 (.046)</td>
</tr>
<tr>
<td>0.56+/-.05 (.022+/-0.002)</td>
<td>0.660 (.026) - # 71</td>
<td>0.91 (.036)</td>
</tr>
<tr>
<td>0.46+/-.05 (.0181+/-0.002)</td>
<td>0.572 (.022) - # 74</td>
<td>0.81 (.032)</td>
</tr>
<tr>
<td>0.37+/-.05 (.0146+/-0.002)</td>
<td>0.457 (.018) - # 77</td>
<td>0.73 (.029)</td>
</tr>
</tbody>
</table>

Note: Refer to appropriate sales drawing for recommended pcb holes and pcb thickness.

PLATING DETAIL FOR COMPLIANT PIN HOLES

Figure 3
Pin Mapping
Figure 4
3.0 HIGH-SPEED ROUTING

3.1 GENERAL ROUTING EXAMPLE (other configurations are possible)

Various routing layers shown separately for clarity
Routing examples shown for reference only
Shown with 0.13mm (0.005") traces and 0.25 mm (0.10") spaces

Figure 5
3.2 HIGH-SPEED TRANSMISSION LINE PLANE

Showing all 4 layers overlaid for a typical single connector
Routing examples shown for reference only
Shown with 0.13mm (0.005”) traces and 0.25 mm (0.10”) spaces

Figure 6
Trace detail typical for all High Speed trace positions

Figure 7
3.3 HIGH-SPEED REFERENCE PLANE ANTI-PAD

Figure 8

See Detail 2
3.4 CONNECTOR PRESS-FIT INTERFACE VIA STUBS

BOTTOM LAUNCH DRIVEN VIA (PREFERRED)

TOP LAUNCH STUB VIA (WORSE CASE)

STANDARD VIA CONFIGURATION
BACK DRILL DEPTH NOT TO EXCEED 1.00mm FROM TOP

Only two annular rings are required for retention of the press-fit via within the printed circuit consequently annular rings on the bottom layer are not needed. Removing the bottom layer annular ring helps minimize the parasitic stub capacitance created by the via.

The anti-pad can be used on other ground layers not shown above. Alternatively, the anti-pad can be made larger with a broader keep-out region on these other ground layers to minimize parasitic capacitance.
3.5 SKEW COMPENSATION

It is recommended that skew compensation be distributed verses grouped in one or more locations.

3.6 TRACE COMPARISON

TRANSITION SHOULD BE SYMMETRIC