Approvals	Name	Date
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Checked By	M.ROCK	2/27/2019
Approved By	M.ROCK	2/27/2019
Released By	Y.GOLDADE	8/27/2018

EC Number	Rev	Submitted By	Date	Approved By	Date
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60923	A	M.ROCK	3/5/19	M.ROCK	3/5/19

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1 Introduction

The following measurements pertain to the following verSI series board mount connector configurations. All measurements use the paste-in-hole (PIH) termination method. The plated thru hole should be back drilled to at least the pin length to optimize signal integrity performance as in Figure 5 - PIH PCB Cross Section with Recommended Back Drill for Best High Speed Performance .

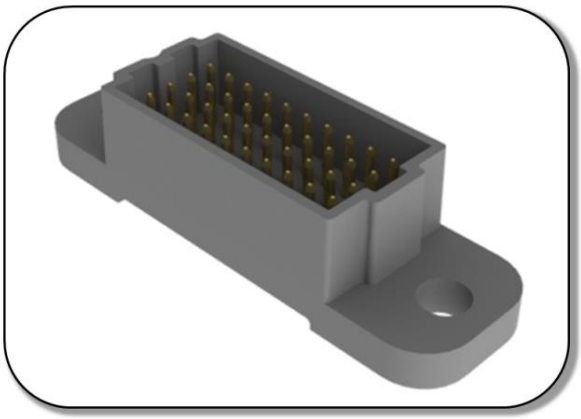


Figure 1 - VSM-xx-xx-80-50-01x - Image

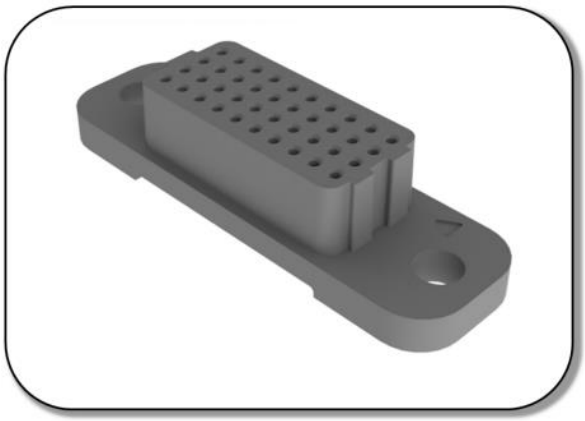


Figure 2 - VSF-xx-xx-50-01-x - Image

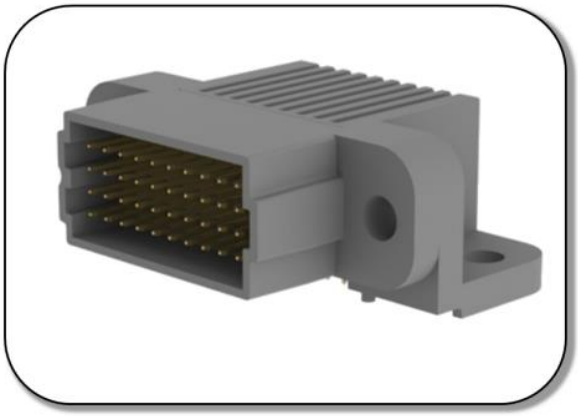


Figure 3 - VSRAM-xx-xx-50-01-x - Image

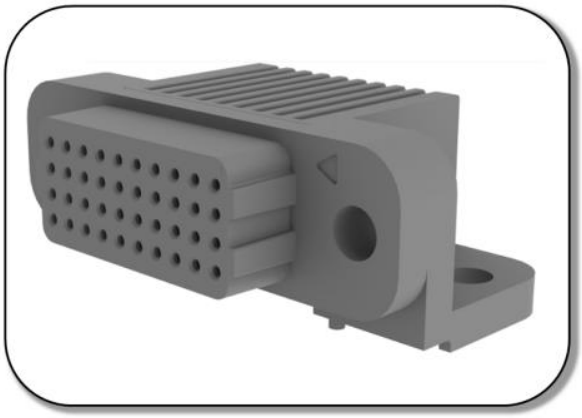


Figure 4 - VSRAF-xx-xx-50-01-x - Image

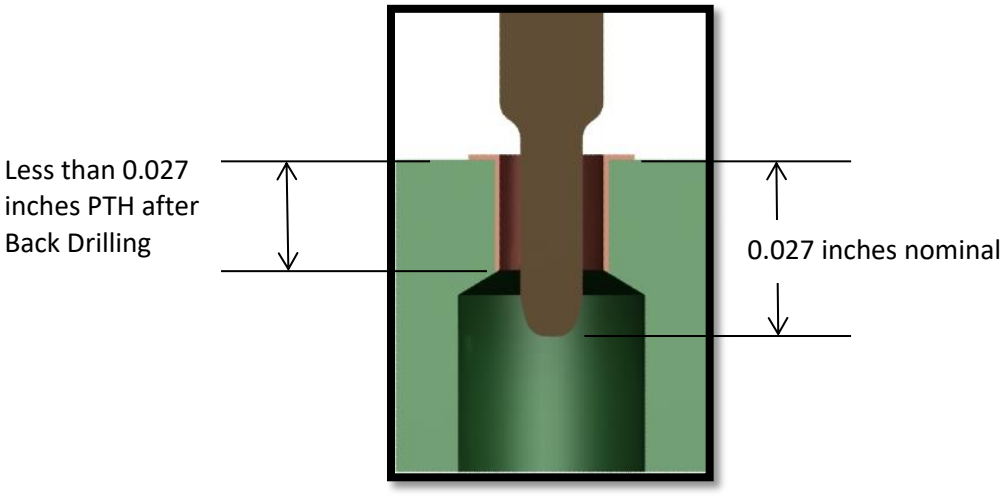
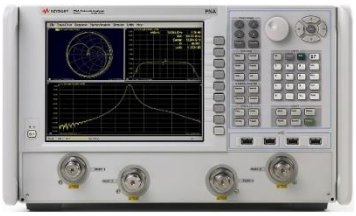


Figure 5 - PIH PCB Cross Section with Recommended Back Drill for Best High Speed Performance

2 Measurement Equipment and Procedures

- *All s-parameter measurements were performed on Keysight PNA N5225A*



- *All 4 singles ended ports on the PNA were calibrated with the Keysight N4692A Electronic Calibration Module(E-Cal)*

- *All measurements were analyzed with Keysight Physical Layer Test System (PLTS) 2016*
- *Differential logical Port 1 – (Port 1 – Port 3)*
- *Differential logical Port 2– (Port 2 – Port 4)*
- *The Measurement setup contains an SMA launch and a section of PCB trace with paste-in-hole (PIH) terminations to the verSI connector.*
- *All Test Fixtures include an 1X-Thru Open and 2x-Thru for fixture de-embedding*
- *PLTS Automatic Fixture Removal (AFR) tool is used to de-embed the SMA connectors and 50 ohm traces up to the mated connector thru hole.*
- *The calibration reference plain is then located at the PCB thru hole where the PIH verSI pin is located*
- *All unused links are 50 ohm load terminated on the near and far ends*

3 verSI Series Open Pin Field Pin-Out Options

G – Ground Pin
P – Positive Differential Pin
N – Negative Differential Pin
S – Signal Pin

Option #3

Differential: High Bandwidth - High Isolation

	1	2	3	4	5	6	7	8	9	10	…
A	G	G	G	G	P	N	G	G	G	G	
B	G	P	N	G	G	G	G	P	N	G	
C	G	G	G	G	P	N	G	G	G	G	
D	G	P	N	G	G	G	G	P	N	G	
…											

Figure 6 - Pinout Option #3, Differential: High Bandwidth - High Isolation

Option #2

Differential: Medium Bandwidth - Medium Isolation

	1	2	3	4	5	6	7	8	9	10	…
A	P	N	G	G	P	N	G	G	P	N	
B	G	G	P	N	G	G	P	N	G	G	
C	P	N	G	G	P	N	G	G	P	N	
D	G	G	P	N	G	G	P	N	G	G	
…											

Figure 7 - Pinout Option #2, Differential: Medium Bandwidth - Medium Isolation

G – Ground Pin
P – Positive Differential Pin
N – Negative Differential Pin
S – Signal Pin

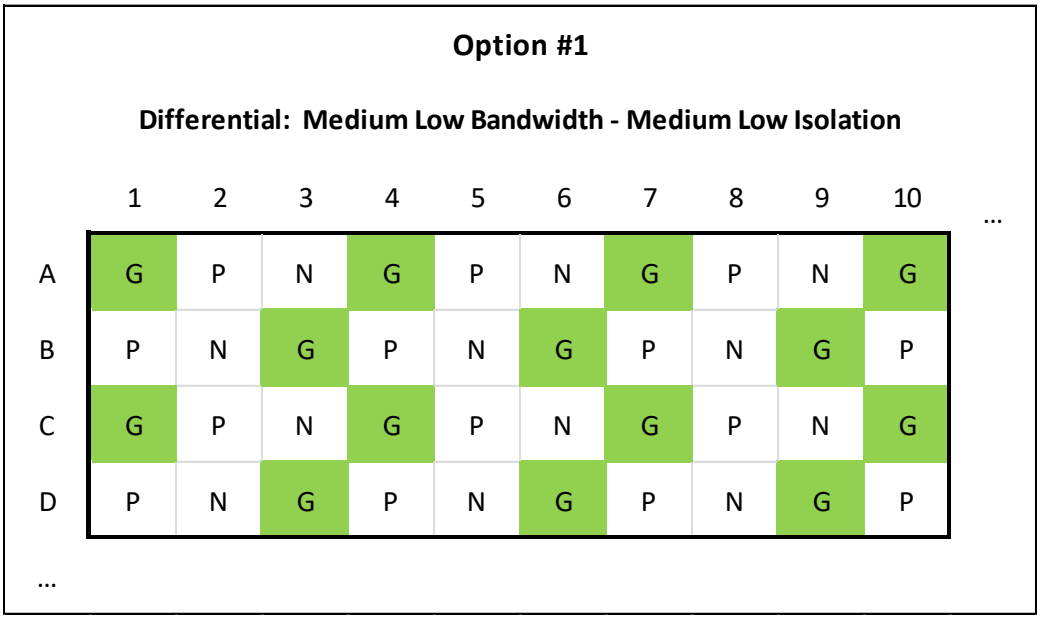


Figure 8 - Pinout Option #1, Differential: Medium Low Bandwidth - Medium Low Isolation

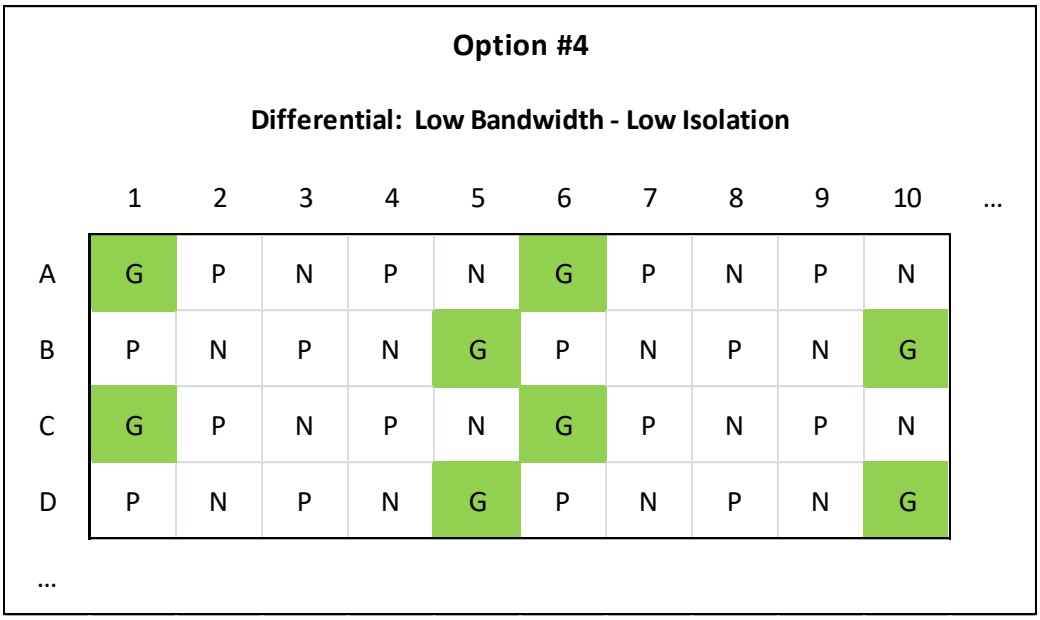


Figure 9 - Pinout Option #4, *Differential: Low* Bandwidth - *Low Isolation*

4 Measured SI Performance - Pin-Out Option #3

4.1 VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x / Pinout #3

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair B2/B3. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

4.1.1 S-Parameter Summary

Parameter	VSM-xx-xx-80-50-01-x / VSF-xx-xx-50-01-x, Option#3 Typical Mated Performance		
Insertion Loss	-0.1 dB @ 5.0 GHz	-0.6 dB @ 10.0 GHz	-3.0 dB @ 20.7 GHz
Return Loss	-35.9 dB @ 5.0 GHz	-13.7 dB @ 10.0 GHz	-10.3 dB @ 20.7 GHz
Pair to Pair Near-End Crosstalk	-59.0 dB @ 5.0 GHz	-29.7 dB @ 10.0 GHz	-25.8 dB @ 20.7 GHz
Pair to Pair Far-End Crosstalk	-65.9 dB @ 5.0 GHz	-35.0 dB @ 10.0 GHz	-36.8 dB @ 20.7 GHz
Differential Mode to Common Mode Conversion	-35.9 dB @ 5.0 GHz	-33.0 dB @ 10.0 GHz	-17.1 dB @ 20.7 GHz
Propagation Delay	75 ps		
Differential Skew	< 2 ps		

Table 1 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #3 S-Parameter Pair B2/B3 Summary

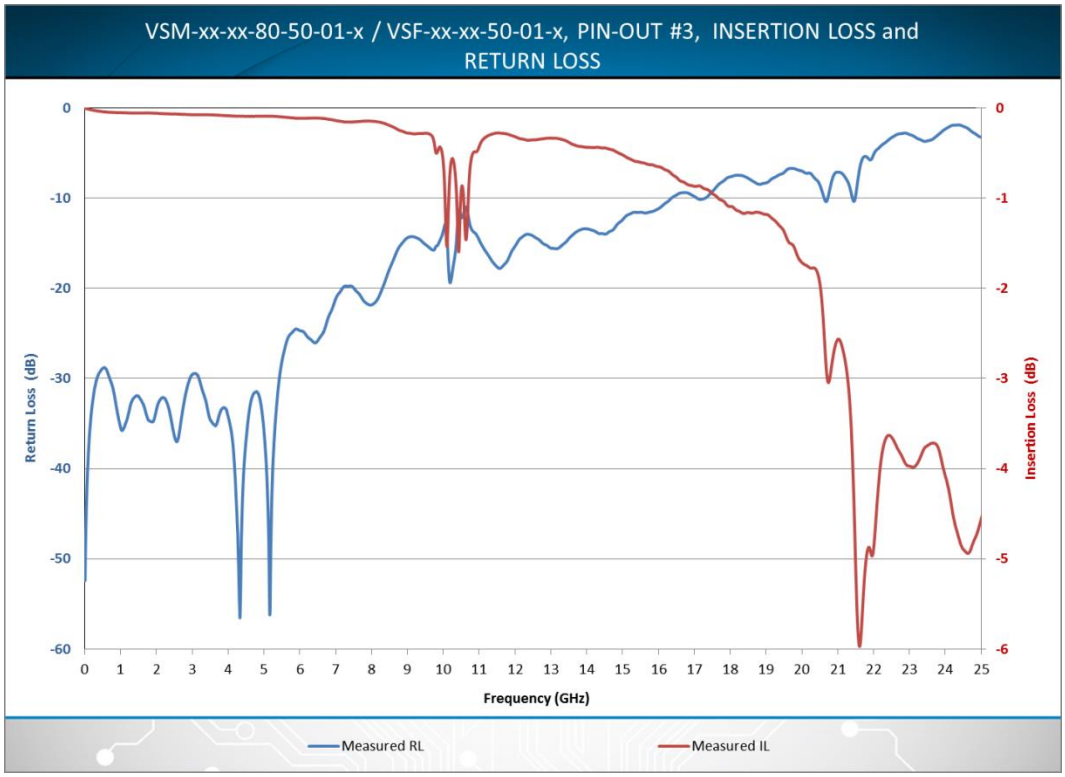


Figure 10 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #3 Insertion Loss/Return Loss

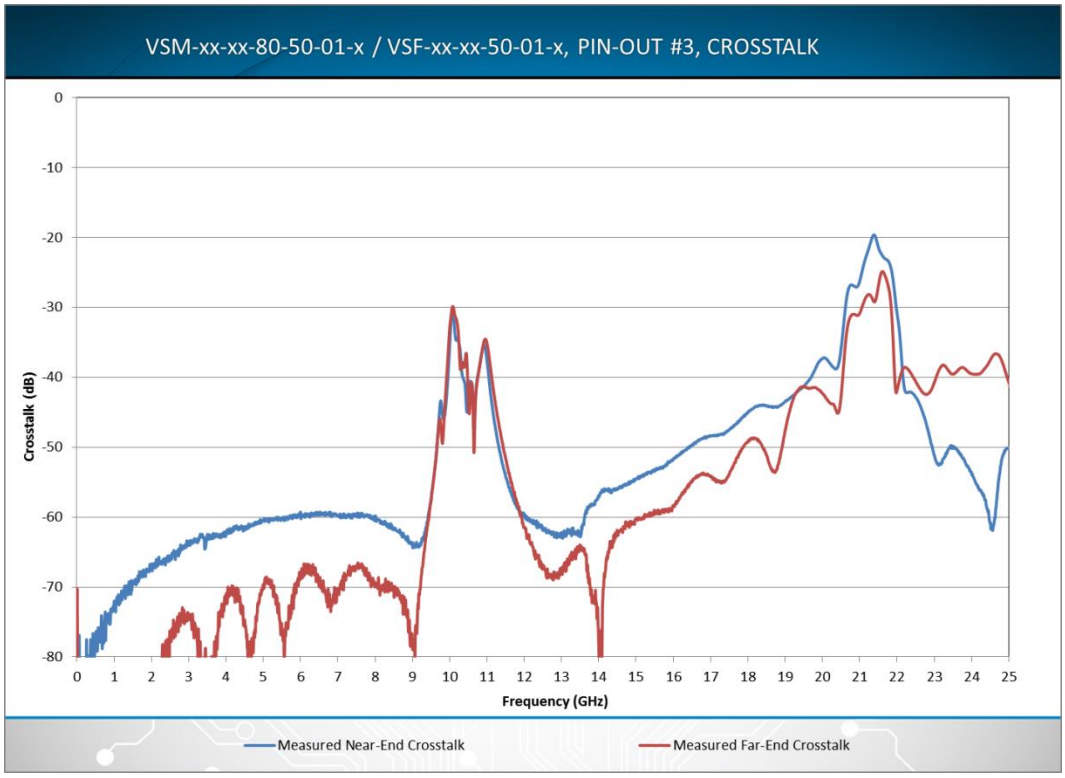


Figure 11 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #3 Crosstalk

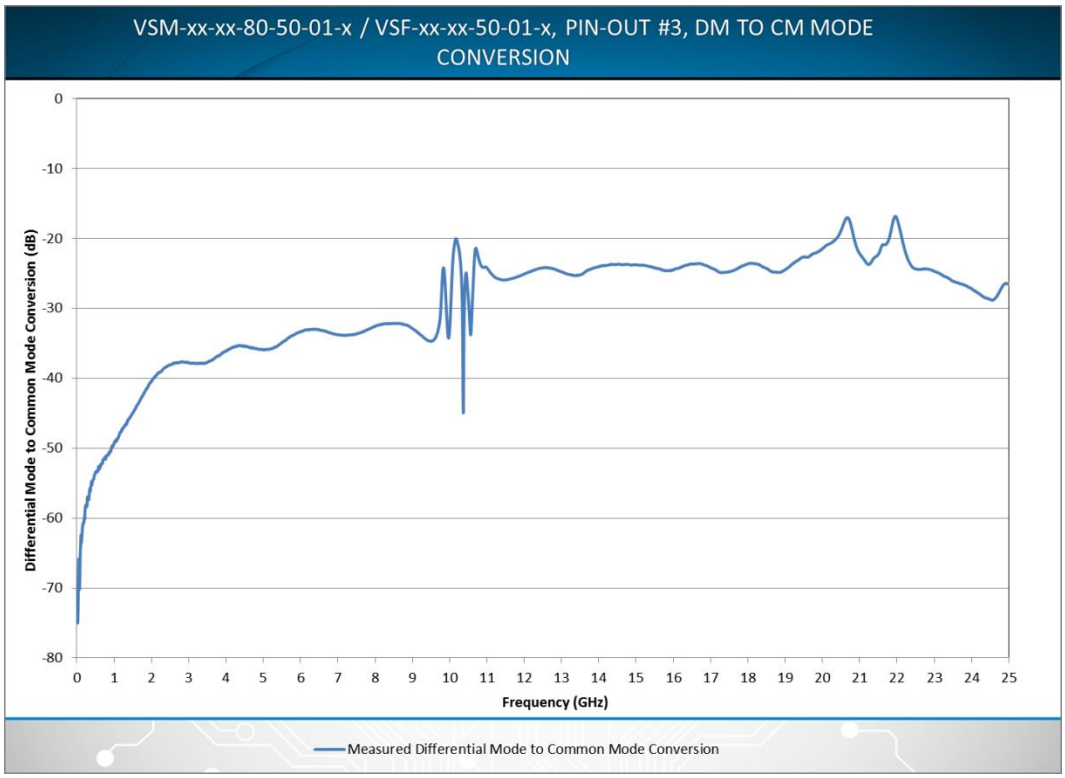


Figure 12 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #3 Mode Conversion

4.1.2 Time Domain Impedance Summary

VSM-xx-xx-80-50-01-x / VSF-xx-xx-50-01-x, Option#2 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 17.5ps	115.1	80.9
Signal Rise Time - 35ps	108.3	94.6
Signal Rise Time - 100ps	104.1	99.7

Table 2 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #3 Impedance Pair B2/B3 Summary

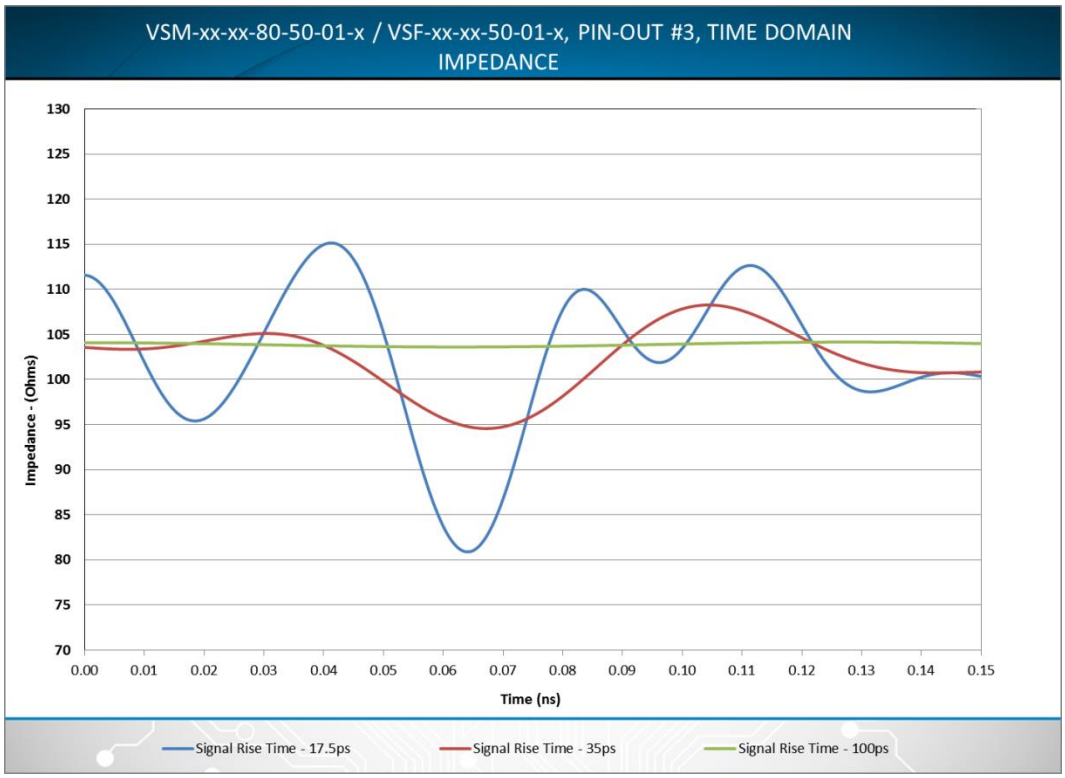


Figure 13 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #3 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

4.2 VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x / Pinout #3

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair B2/B3. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

4.2.1 S-Parameter Summary

Parameter	VSM-xx-xx-80-50-01-x / VSRAF-04-xx-50-01-x, Option#3 Typical Mated Performance		
Insertion Loss	-0.4 dB @ 5.0 GHz	-0.7 dB @ 10.0 GHz	-3.0 dB @ 19.6 GHz
Return Loss	-16.2 dB @ 5.0 GHz	-13.2 dB @ 10.0 GHz	-6.0 dB @ 19.2 GHz
Pair to Pair Near-End Crosstalk	-64.3 dB @ 5.0 GHz	-59.3 dB @ 10.0 GHz	-27.1 dB @ 19.2 GHz
Pair to Pair Far-End Crosstalk	-73.3 dB @ 5.0 GHz	-56.9 dB @ 10.0 GHz	-28.2 dB @ 19.2 GHz
Differential Mode to Common Mode Conversion	-41.2 dB @ 5.0 GHz	-36.4 dB @ 10.0 GHz	-44.3 dB @ 19.2 GHz
Propagation Delay	RowD- 83 ps, RowC- 95ps, RowB- 110ps, RowA - 123ps		
Differential Skew	< 2 ps		

Table 3 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #3, S-Parameter Pair B2/B3 Summary

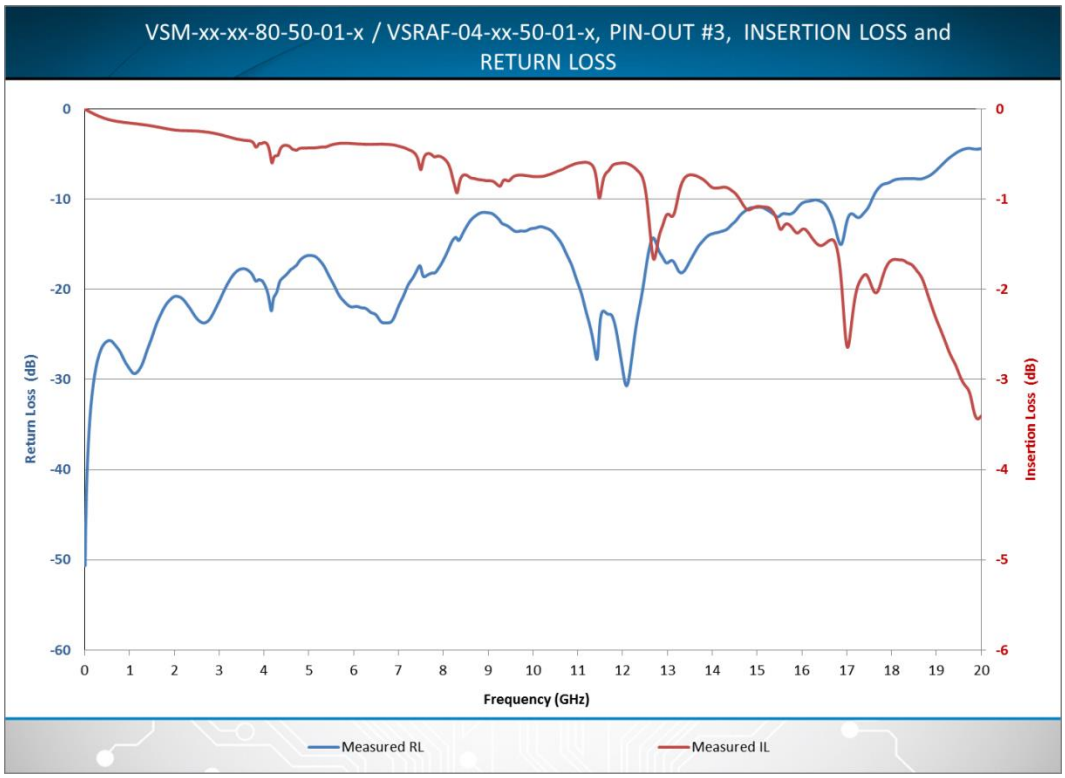


Figure 14 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #3 Insertion Loss/Return Loss

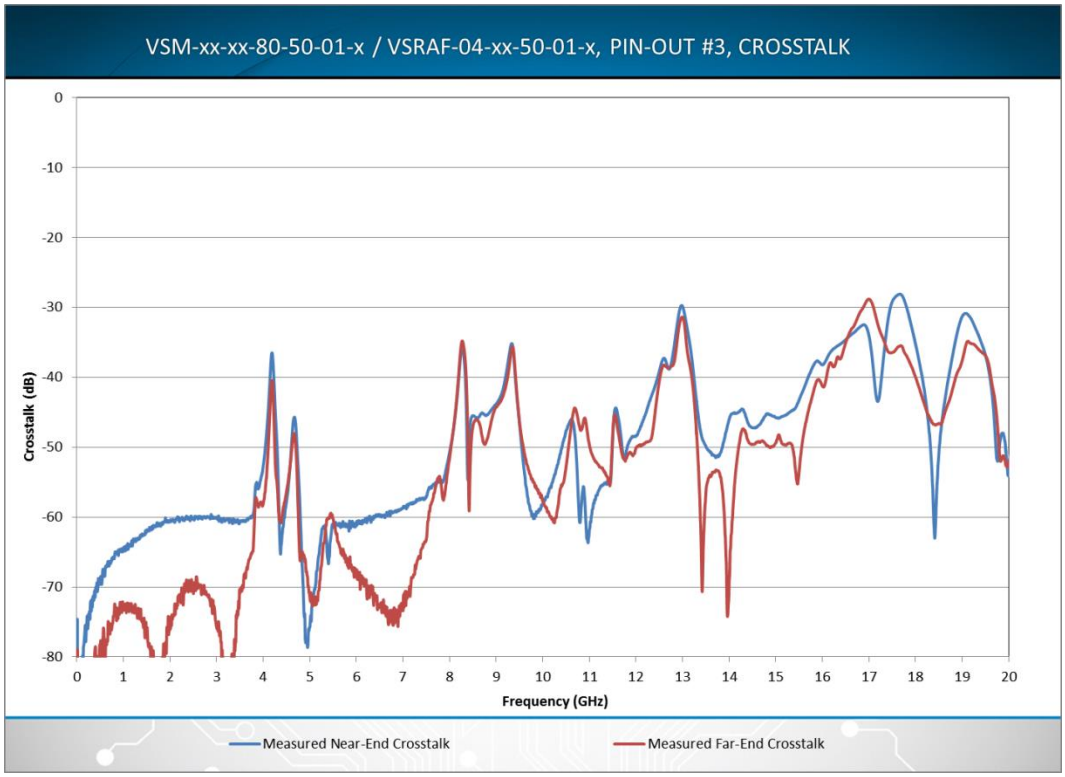


Figure 15 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #3 Crosstalk

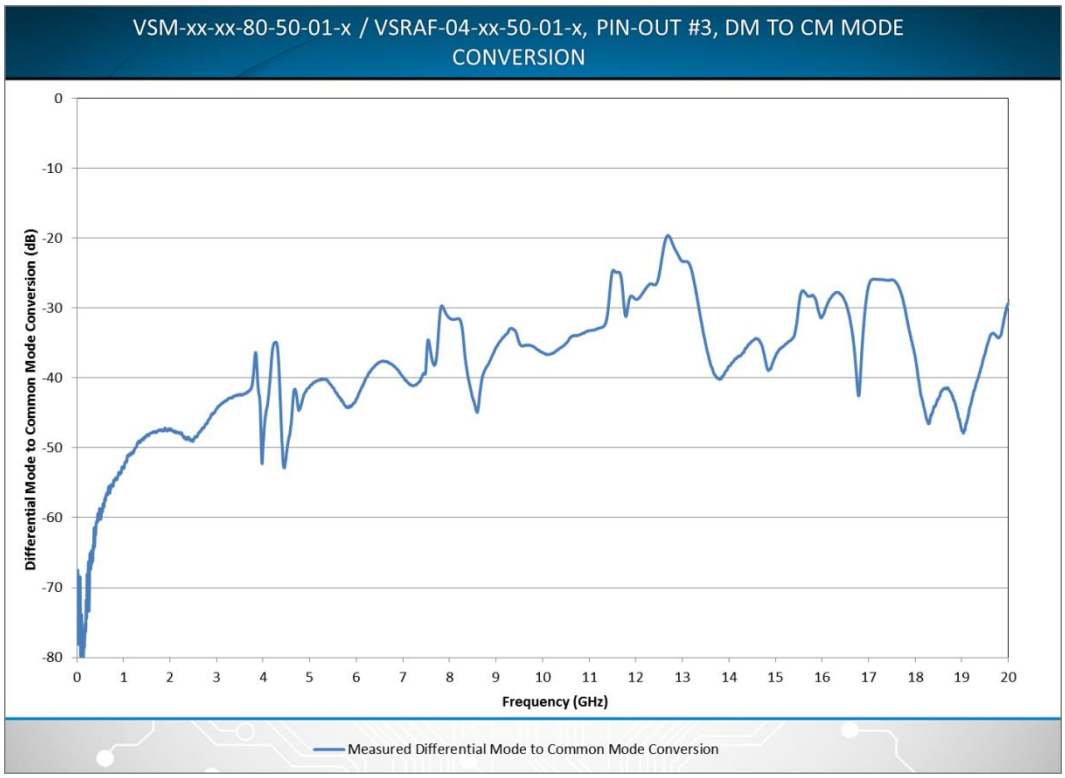


Figure 16 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #3 Mode Conversion

4.2.2 Time Domain Impedance Summary

VSM-xx-xx-80-50-01-x / VSRAF-04-xx-50-01-x, Option#3 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 17.5ps	118.6	78.5
Signal Rise Time - 35ps	115.4	92.2
Signal Rise Time - 100ps	114.6	99.6

Table 4 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #3 Impedance Pair B2/B3 Summary

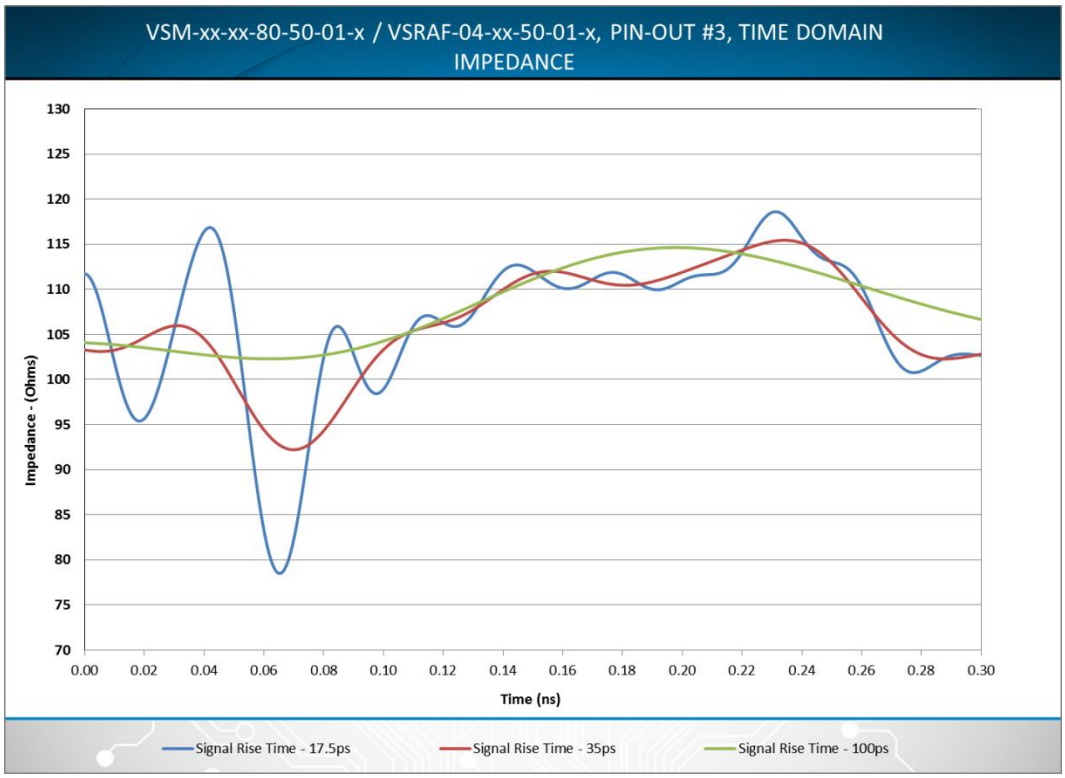


Figure 17 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #3 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

4.3 VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x / Pinout #3

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair B2/B3. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

4.3.1 S-Parameter Summary

Parameter	VSRAM-04-xx-50-01-x / VSRAF-04-xx-50-01-x, Option#3 Typical Mated Performance		
Insertion Loss	-0.9 dB @ 5.0 GHz	-1.6 dB @ 10.0 GHz	-3.0 dB @ 11.2 GHz
Return Loss	-32.2 dB @ 5.0 GHz	-9.5 dB @ 10.0 GHz	-9.0 dB @ 11.2 GHz
Pair to Pair Near-End Crosstalk	-38.1 dB @ 5.0 GHz	-46.4 dB @ 10.0 GHz	-41.4 dB @ 11.2 GHz
Pair to Pair Far-End Crosstalk	-37.6 dB @ 5.0 GHz	-43.3 dB @ 10.0 GHz	-35.4 dB @ 11.2 GHz
Differentail Mode to Common Mode Conversion	-45.6 dB @ 5.0 GHz	-43.6 dB @ 10.0 GHz	-26.1 dB @ 11.2 GHz
Propagation Delay	Row D - 140 ps, Row C - 165ps, Row B - 190ps, Row A - 215ps		
Differential Skew	< 2 ps		

Table 5 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #3 S-Parameter Pair B2/B3 Summary

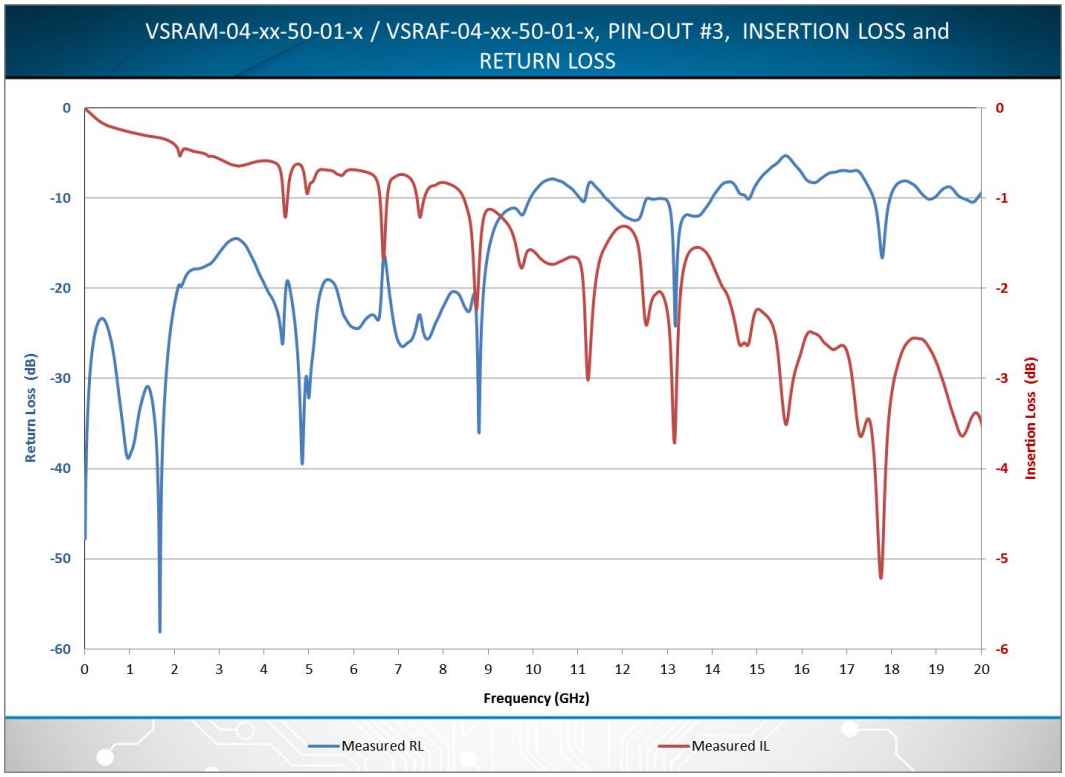


Figure 18 - VSRAM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #3 Insertion Loss/Return Loss

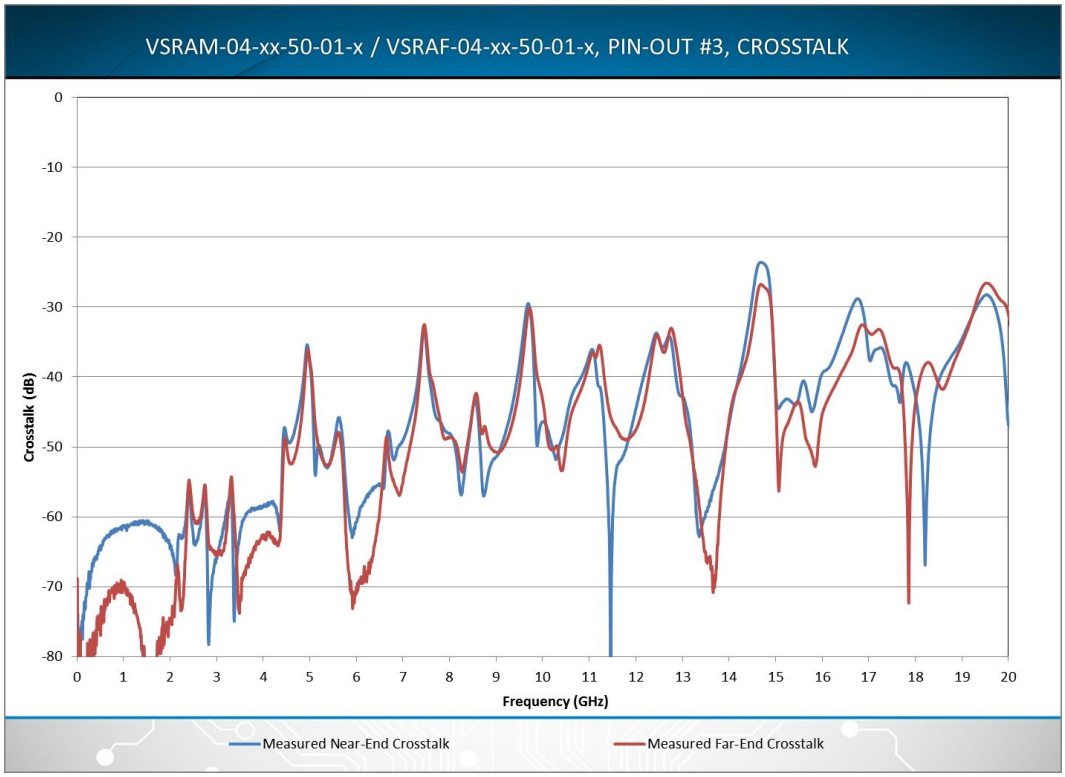


Figure 19 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #3 Crosstalk

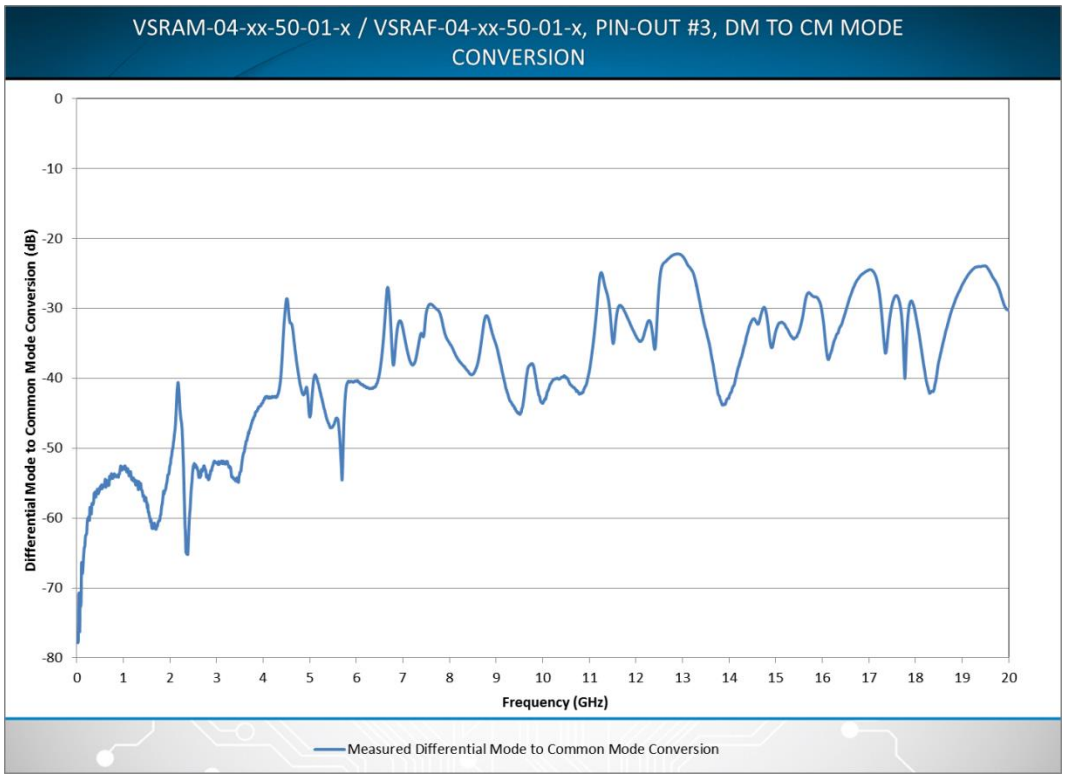


Figure 20 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #3 Mode Conversion

4.3.2 Time Domain Impedance Summary

VSRAM-04-xx-50-01-x / VSRAF-04-xx-50-01-x, Option#3 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 17.5ps	118.6	81.3
Signal Rise Time - 35ps	112.6	92.4
Signal Rise Time - 100ps	112.2	100.0

Table 6 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #3 Impedance Pair B2/B3 Summary

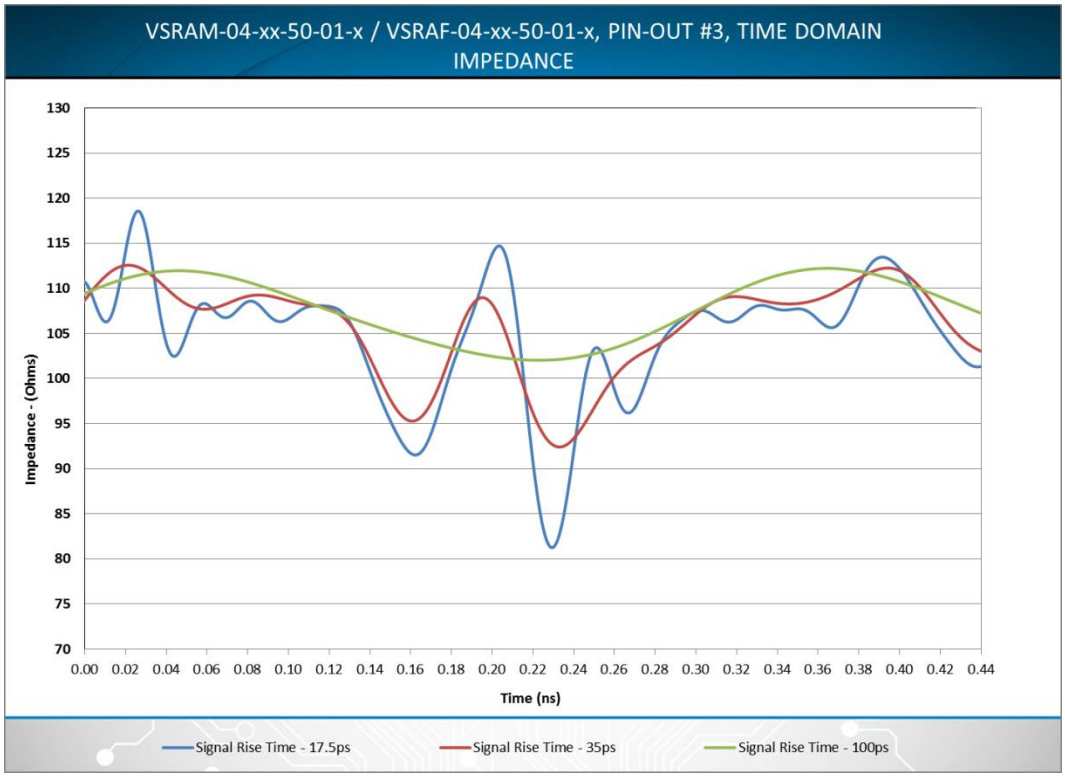


Figure 21 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #3 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

5 Measured SI Performance - Pin-Out Option #2

5.1 VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x / Pinout #2

- Frequency Domain S-Parameter Summary for pin-out option#2 differential pair B3/B4. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

5.1.1 S-Parameter Summary

Parameter	VSM-xx-xx-80-50-01-x / VSF-xx-xx-50-01-x, Option#2 Typical Mated Performance		
Insertion Loss	-0.2 dB @ 5.0 GHz	-0.6 dB @ 10.0 GHz	-3.0 dB @ 16.8 GHz
Return Loss	-38.2 dB @ 5.0 GHz	-19.5 dB @ 10.0 GHz	-6.0 dB @ 16.0 GHz
Pair to Pair Near-End Crosstalk	-46.8 dB @ 5.0 GHz	-45.2 dB @ 10.0 GHz	-26.9 dB @ 16.0 GHz
Pair to Pair Far-End Crosstalk	-47.6 dB @ 5.0 GHz	-29.2 dB @ 10.0 GHz	-24.2 dB @ 16.0 GHz
Differential Mode to Common Mode Conversion	-53.8 dB @ 5.0 GHz	-25.8 dB @ 10.0 GHz	-22.1 dB @ 16.0 GHz
Propagation Delay	75 ps		
Differential Skew	< 2 ps		

Table 7 - VSM-xx-xx-50-01-x / VSF-xx-xx-50-01-x - #2 S-Parameter Pair B3/B4 Summary

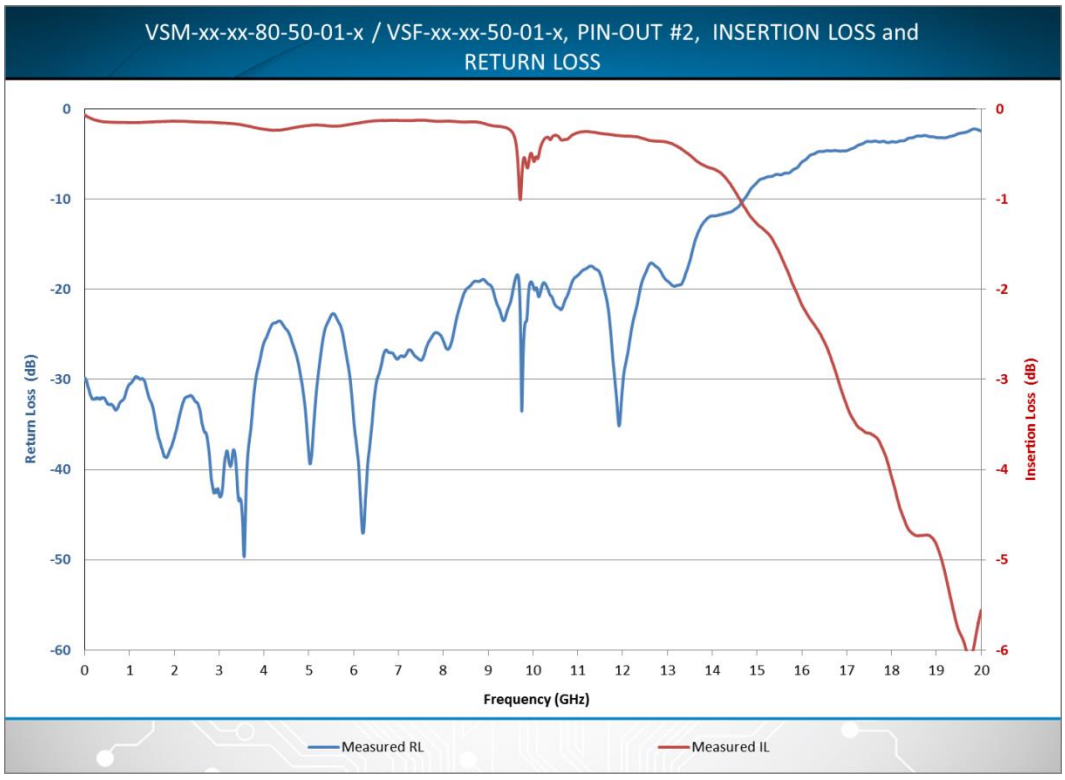


Figure 22 - VSM-xx-xx-50-01-x / VSF-xx-xx-50-01-x - #2 Insertion Loss/Return Loss

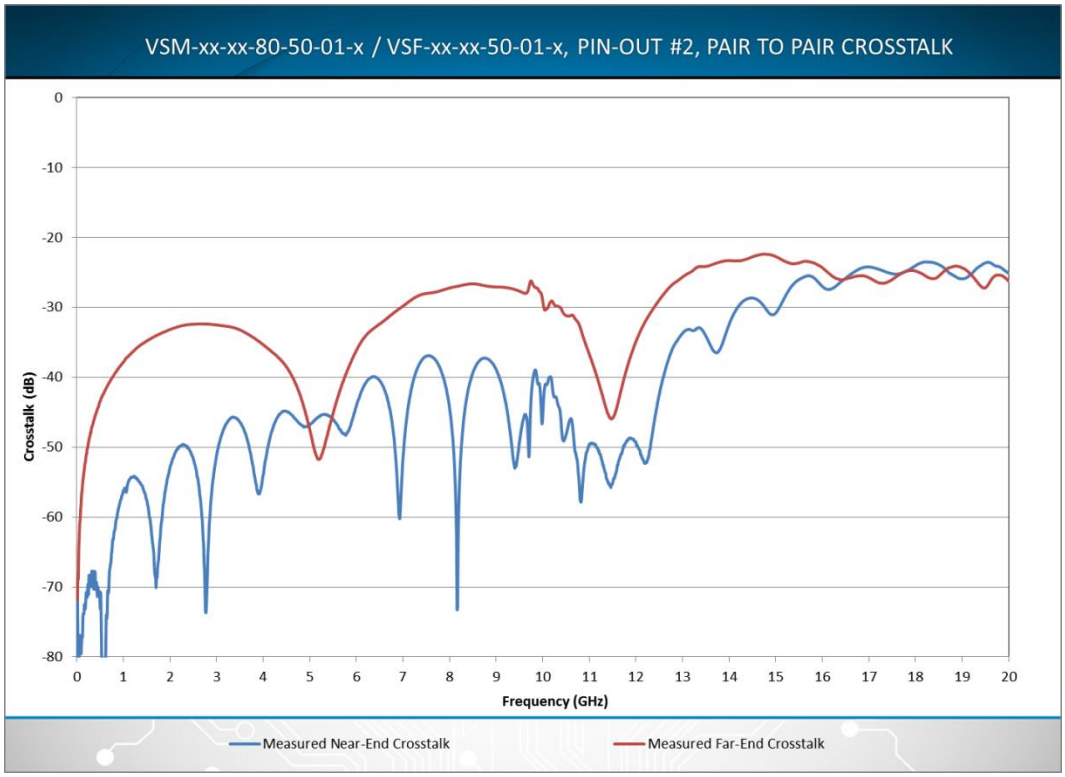


Figure 23 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #2 Crosstalk

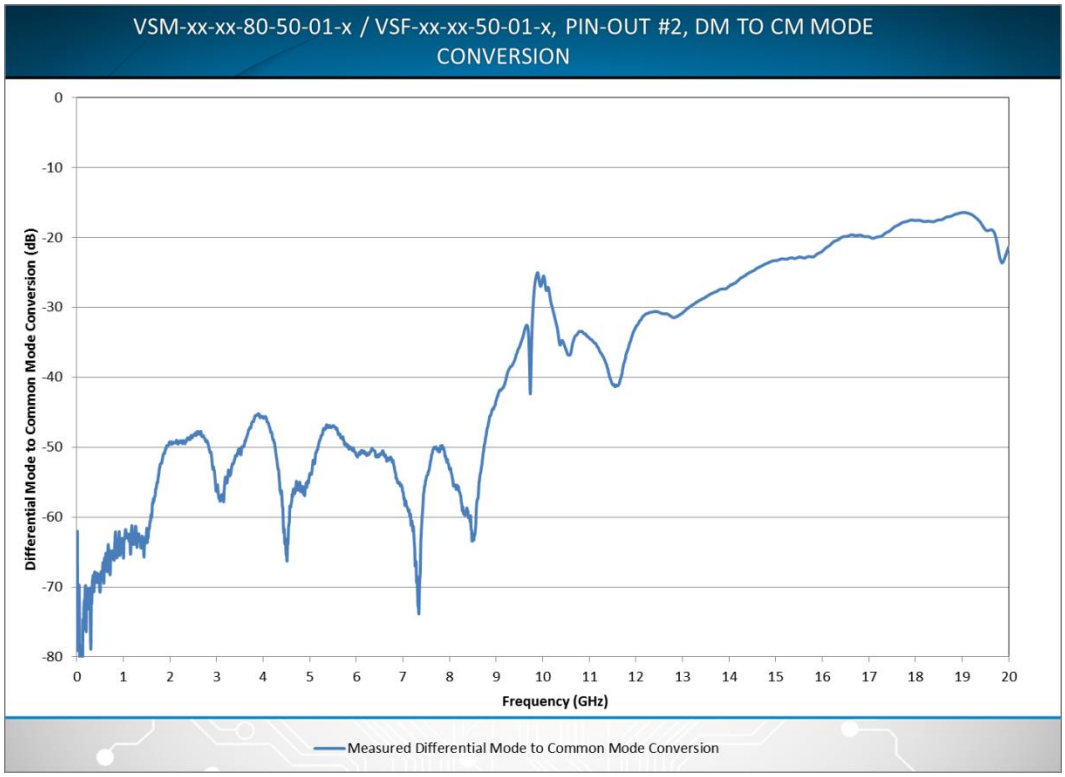


Figure 24 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #2 Mode Conversion

5.1.2 Time Domain Impedance Summary

VSM-xx-xx-80-50-01-x / VSF-xx-xx-50-01-x, Option#2 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 17.5ps	119.5	84.3
Signal Rise Time - 35ps	107.4	95.1
Signal Rise Time - 100ps	101.2	100.4

Table 8 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #2 Impedance Pair B3/B4 Summary

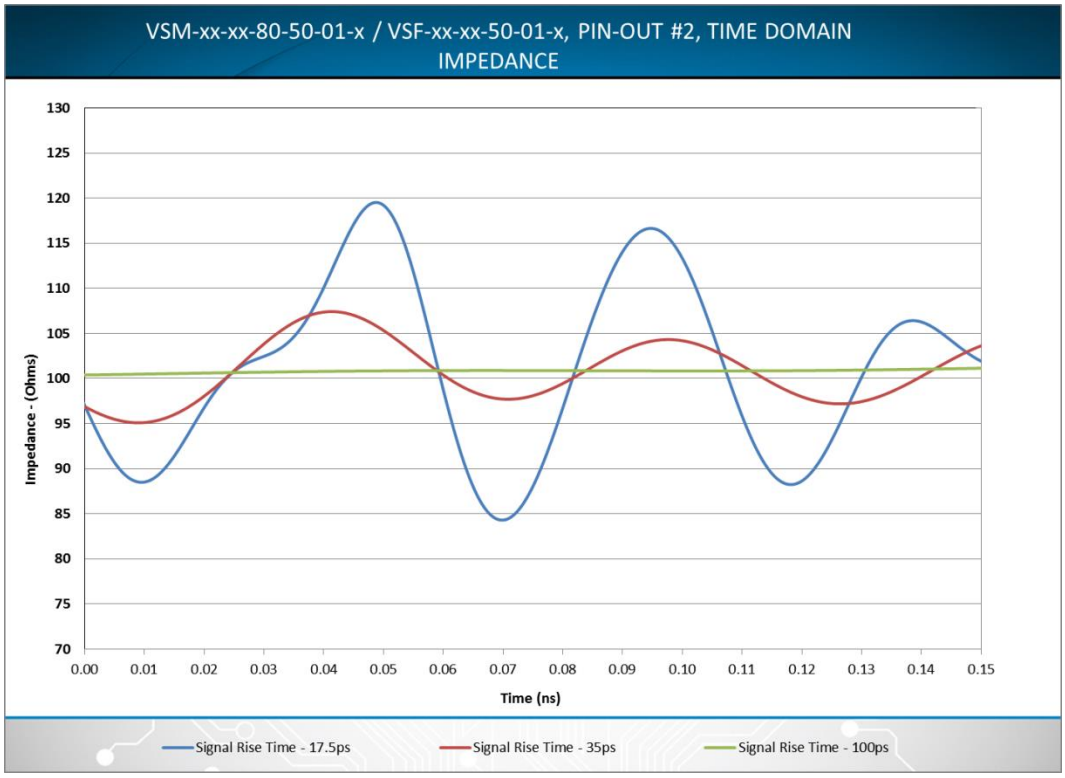


Figure 25 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #2 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x / Pinout #2

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair B3/B4. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

5.1.3 S-Parameter Summary

Parameter	VSM-04-xx-80-50-01-x / VSRAF-04-xx-50-01-x, Option#2 Typical Mated Performance		
Insertion Loss	-0.4 dB @ 5.0 GHz	-0.6 dB @ 10.0 GHz	-3.0 dB @ 15.2 GHz
Return Loss	-22.5 dB @ 5.0 GHz	-14.5 dB @ 10.0 GHz	-5.9 dB @ 15.2 GHz
Pair to Pair Near-End Crosstalk	-45.1 dB @ 5.0 GHz	-33.8 dB @ 10.0 GHz	-32.4 dB @ 15.2 GHz
Pair to Pair Far-End Crosstalk	-46.2 dB @ 5.0 GHz	-42.3 dB @ 10.0 GHz	-38.0 dB @ 15.2 GHz
Differentail Mode to Common Mode Conversion	-68.8 dB @ 5.0 GHz	-38.5 dB @ 10.0 GHz	-25.2 dB @ 15.2 GHz
Propagation Delay	Row D - 83 ps, Row C - 96ps, Row B - 110ps, Row A - 123ps		
Differential Skew	< 2 ps		

Table 9 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #2 S-Parameter Pair C5/C6 Summary

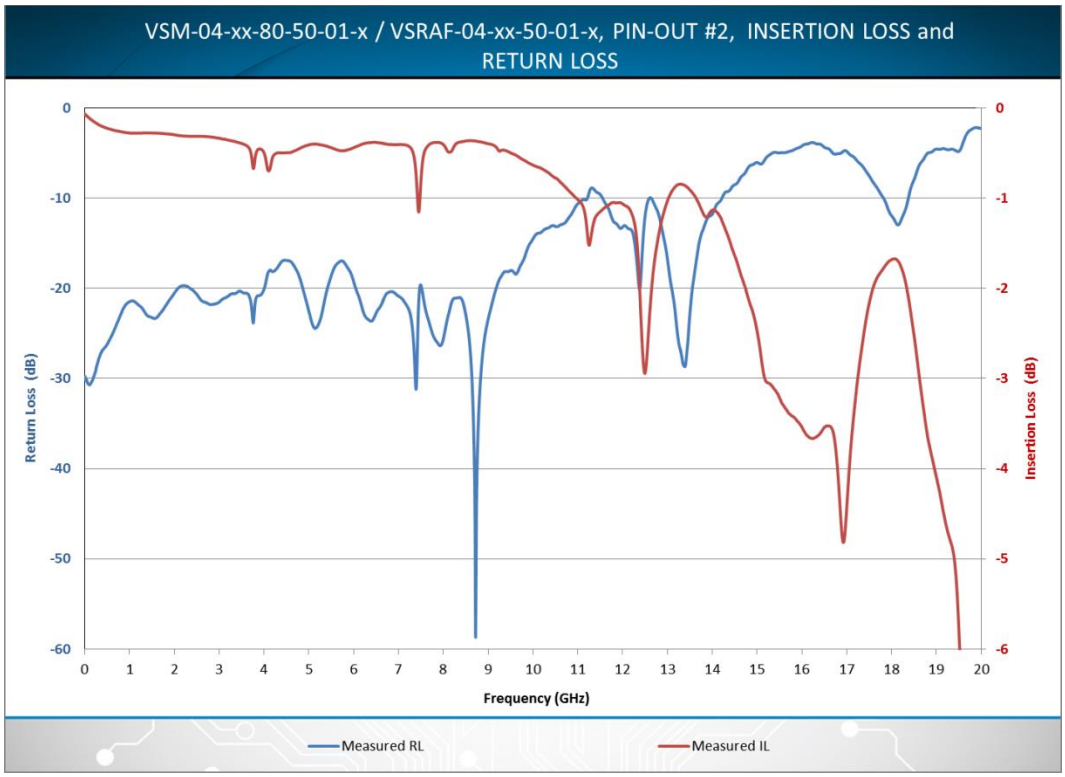


Figure 26 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #2 Insertion Loss/Return Loss

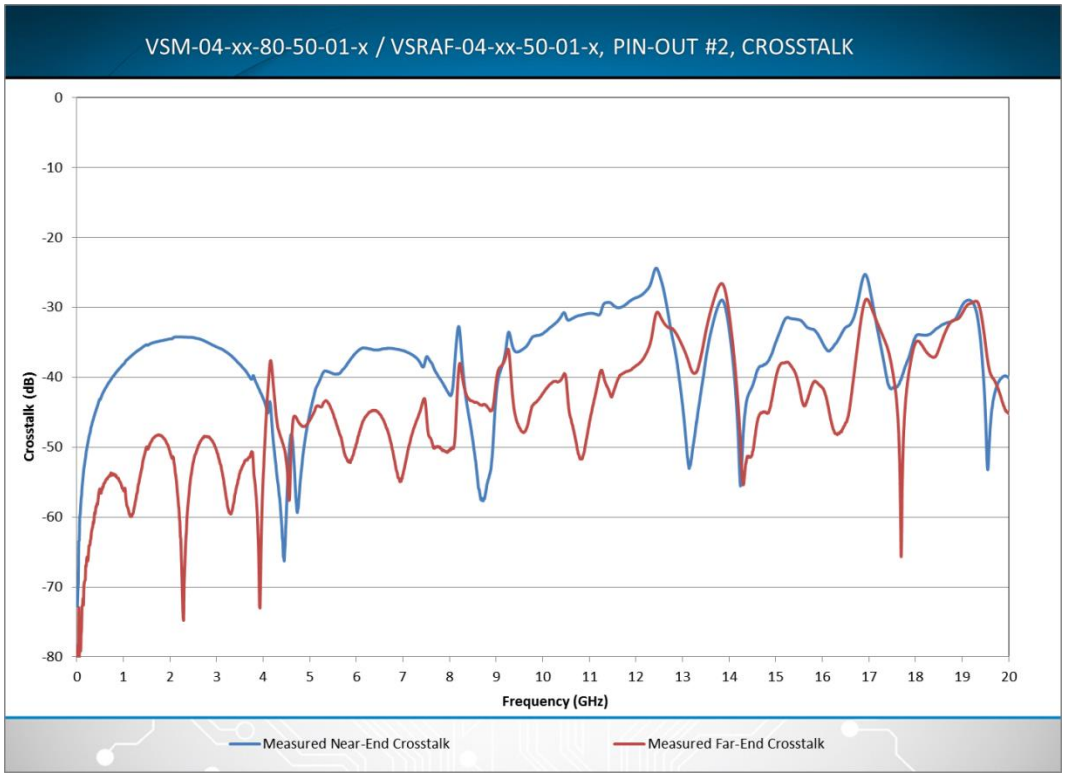


Figure 27 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #2 Crosstalk

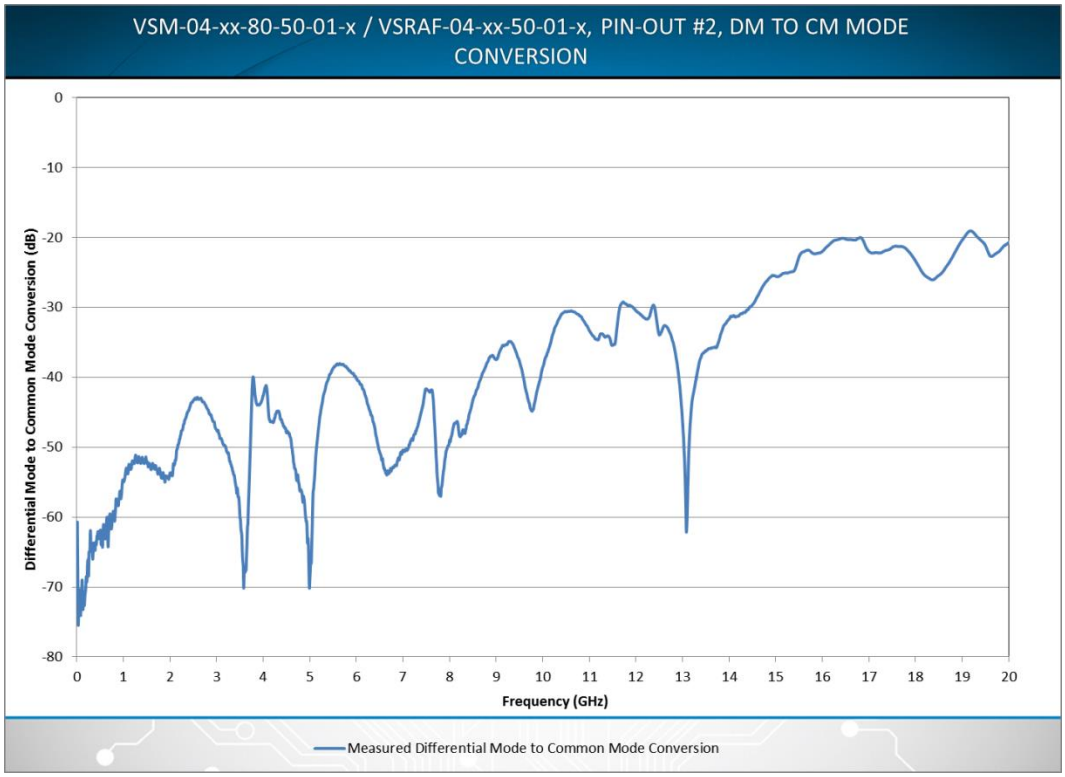


Figure 28 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #2 Mode Conversion

5.1.4 Time Domain Impedance Summary

VSM-04-xx-80-50-01-x / VSRAF-04-xx-50-01-x, Option#2 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 17.5ps	122.0	84.3
Signal Rise Time - 35ps	117.2	95.1
Signal Rise Time - 100ps	113.0	100.4

Table 10 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #2 Impedance Pair C5/C6 Summary

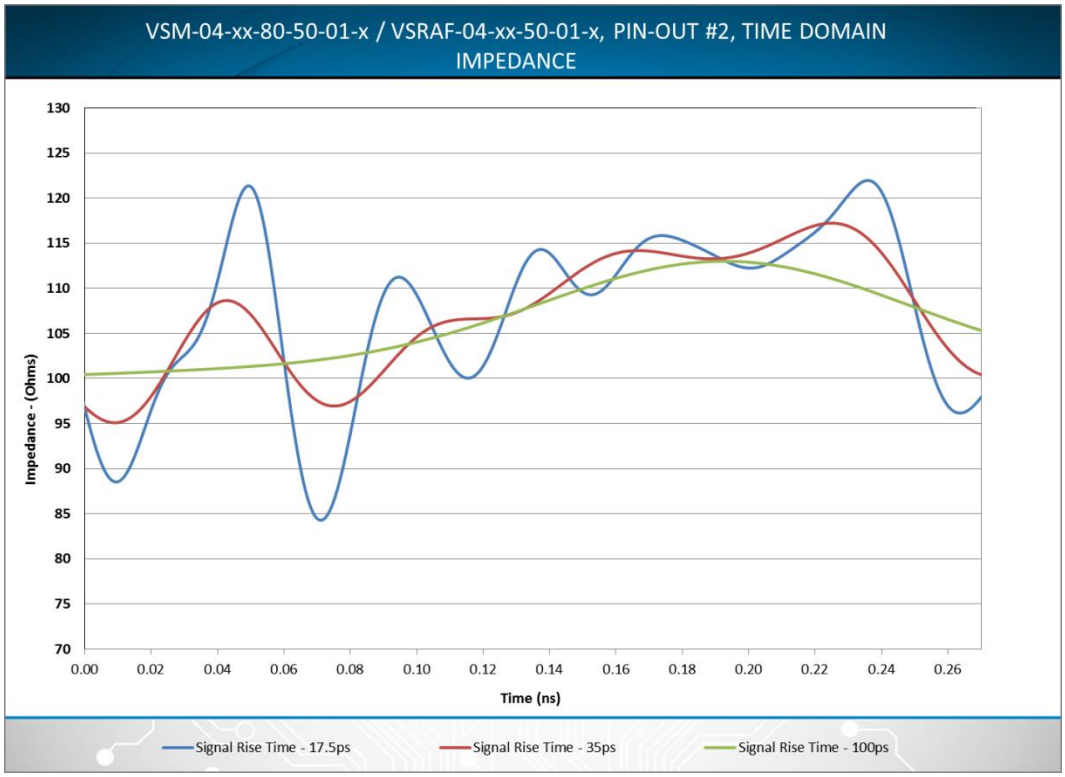


Figure 29 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #2 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

5.2 VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x / Pinout #2

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair B3/B4. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

5.2.1 S-Parameter Summary

Parameter	VSRAM-04-xx-50-01-x / VSRAF-04-xx-50-01-x, Option#2 Typical Mated Performance		
Insertion Loss	-0.8 dB @ 5.0 GHz	-1.0 dB @ 10.0 GHz	-3.0 dB @ 12.3 GHz
Return Loss	-18.6 dB @ 5.0 GHz	-16.5 dB @ 10.0 GHz	-11.9 dB @ 12.3 GHz
Pair to Pair Near-End Crosstalk	-30.2 dB @ 5.0 GHz	-33.8 dB @ 10.0 GHz	-33.6 dB @ 12.3 GHz
Pair to Pair Far-End Crosstalk	-44.5 dB @ 5.0 GHz	-30.9 dB @ 10.0 GHz	-31.9 dB @ 12.3 GHz
Differential Mode to Common Mode Conversion	-43.4 dB @ 5.0 GHz	-34.7 dB @ 10.0 GHz	-25.9 dB @ 12.3 GHz
Propagation Delay	Row D - 140ps, Row C - 165ps, Row B - 190ps, Row A - 215ps		
Differential Skew	< 2 ps		

Table 11 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #2 S-Parameter Pair B3/B4 Summary

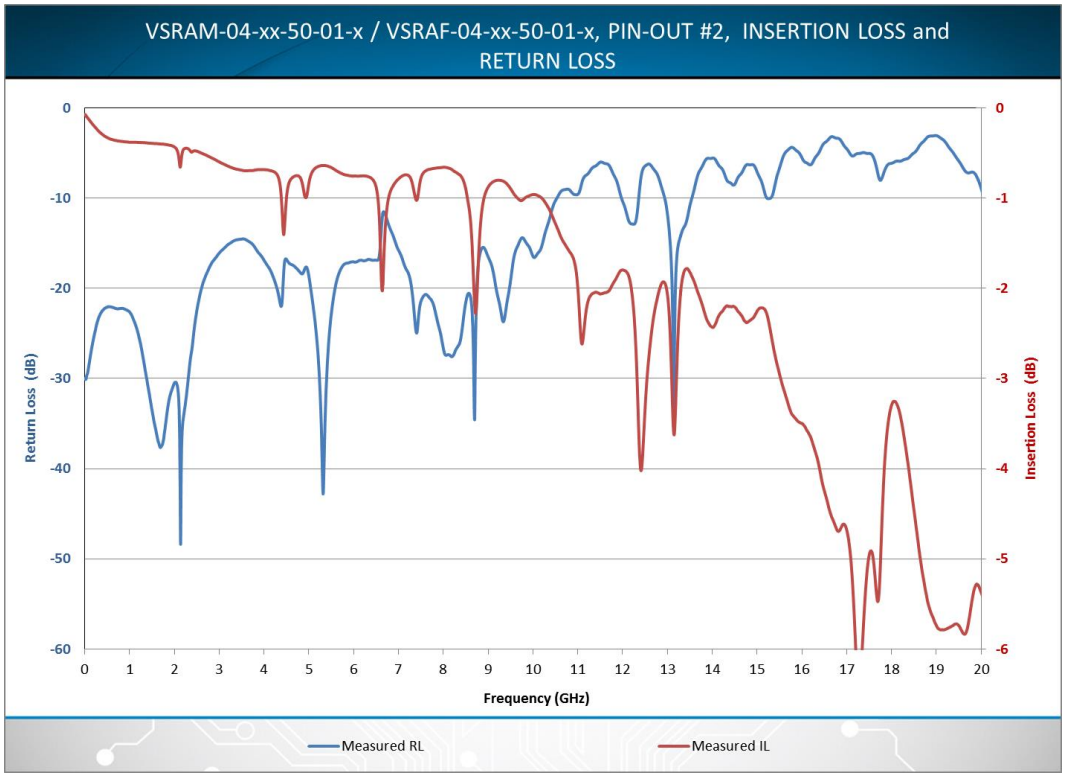


Figure 30 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #2 Insertion Loss/Return Loss

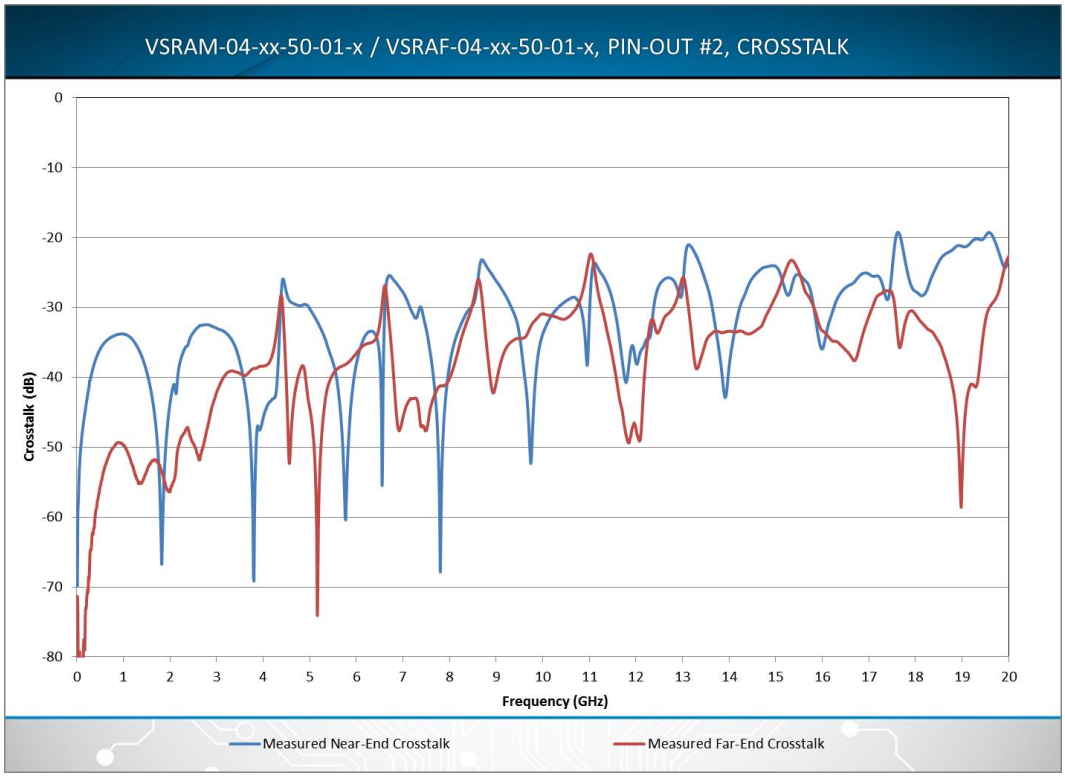


Figure 31 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #2 Crosstalk

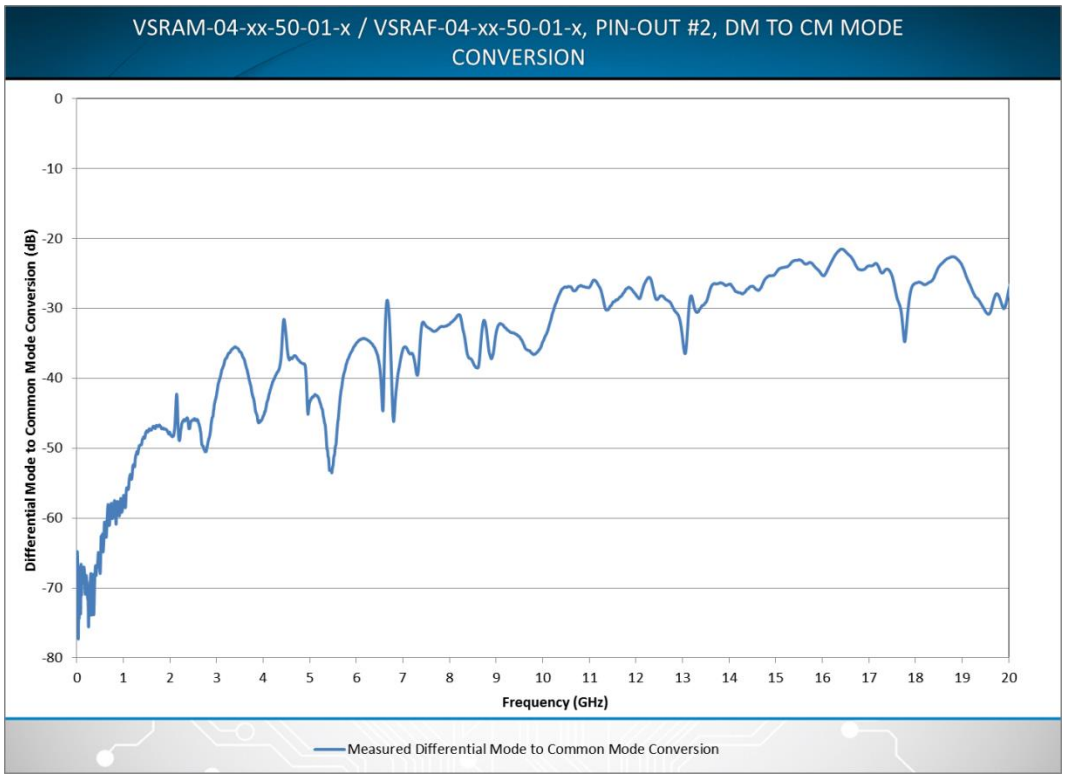


Figure 32 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #2 Mode Conversion

5.2.2 Time Domain Impedance Summary

VSRAM-04-xx-50-01-x / VSRAF-04-xx-50-01-x, Option#2 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 17.5ps	123.1	86.5
Signal Rise Time - 35ps	114.2	96.5
Signal Rise Time - 100ps	112.2	103.9

Table 12 - VSRAM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #2 Impedance Pair B3/B4 Summary

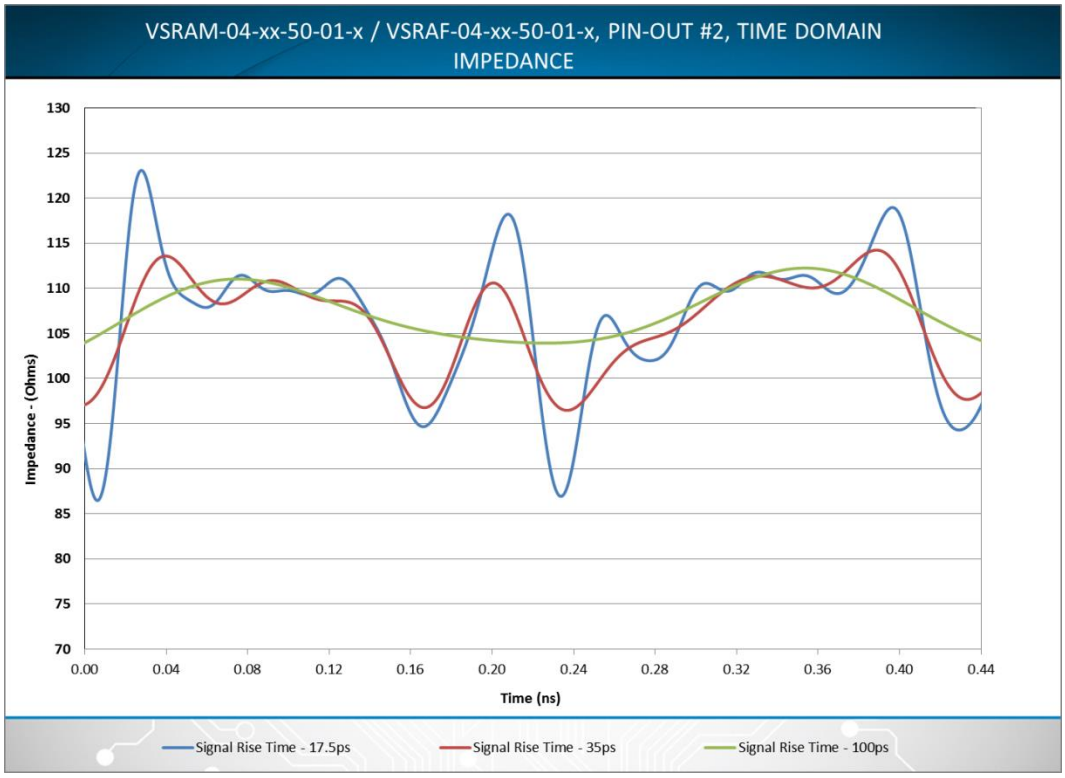


Figure 33 - VSRAM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #2 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

6 Measured SI Performance - Pin-Out Option #1

6.1 VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x / Pinout #1

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair B4/B5. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

6.1.1 S-Parameter Summary

Parameter	VSM-xx-xx-80-50-01-x / VSF-xx-xx-50-01-x, Option#1 Typical Mated Performance	
Insertion Loss	-1.0 dB @ 5.0 GHz	-1.1 dB @ 10.0 GHz
Return Loss	-13.1 dB @ 5.0 GHz	-7.2 dB @ 10.0 GHz
Pair to Pair Near-End Crosstalk	-29.4 dB @ 5.0 GHz	-29.6 dB @ 10.0 GHz
Pair to Pair Far-End Crosstalk	-36.7 dB @ 5.0 GHz	-33.0 dB @ 10.0 GHz
Differential Mode to Common Mode Conversion	-24.8 dB @ 5.0 GHz	-15.2 dB @ 10.0 GHz
Propagation Delay	75 ps	
Differential Skew	< 2 ps	

Table 13 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #1 S-Parameter Pair B4/B5 Summary

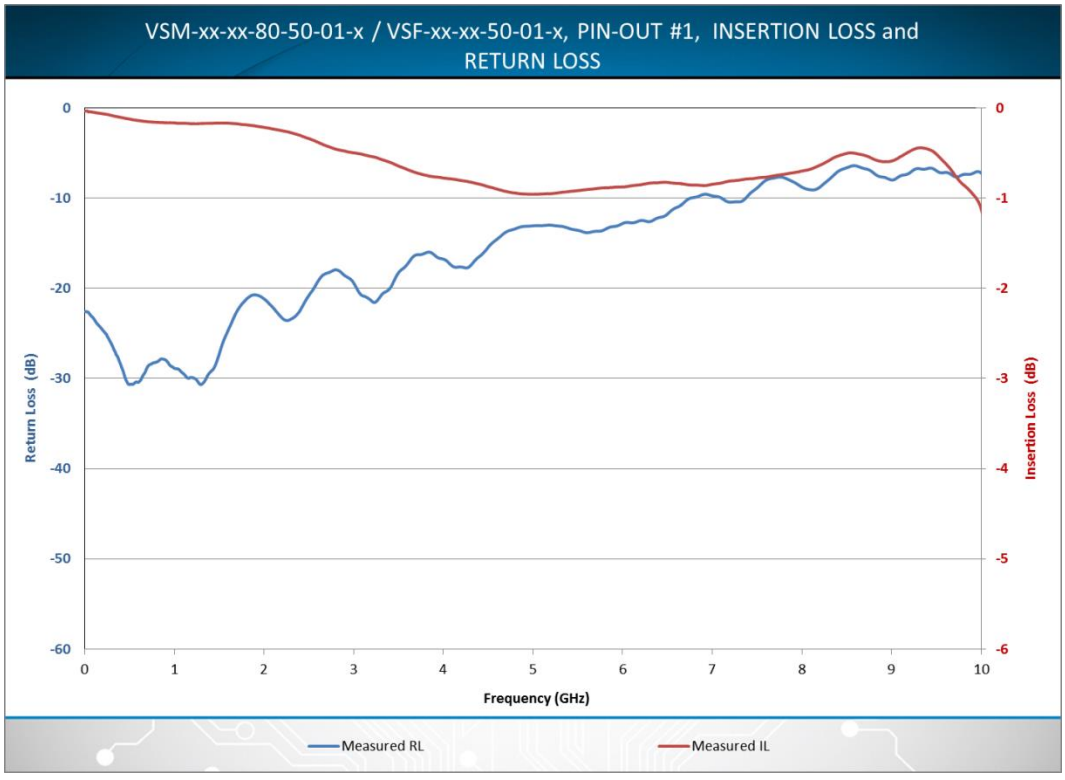


Figure 34 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #1 Insertion Loss/Return Loss

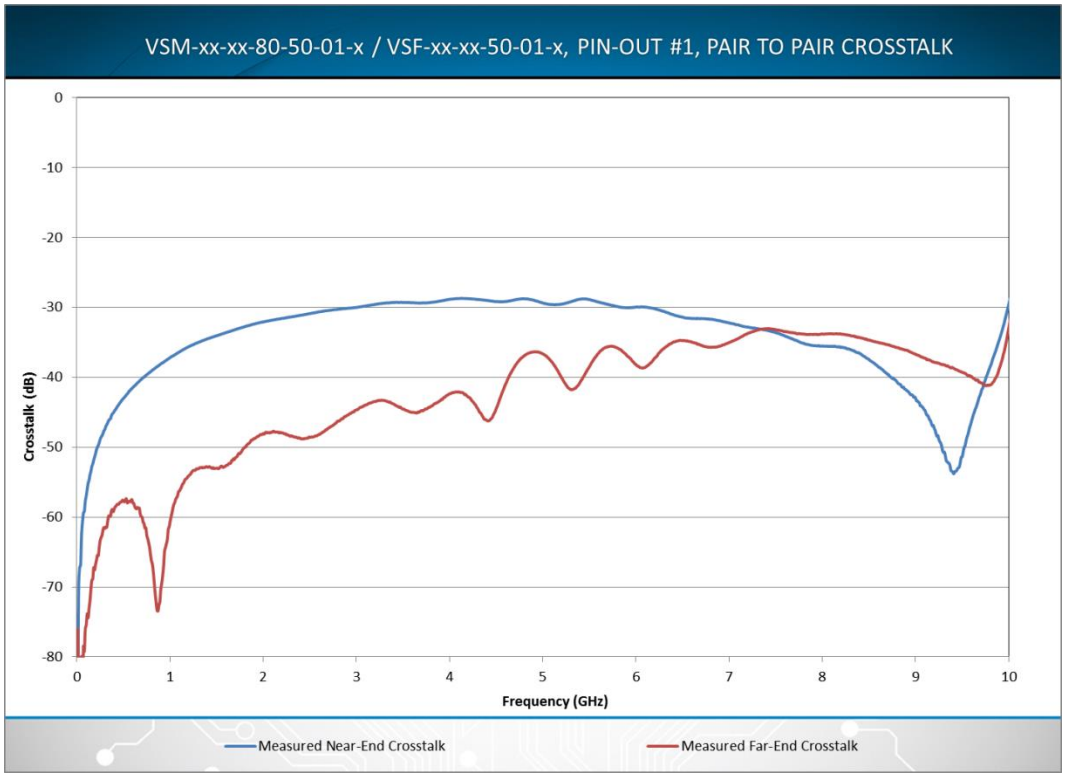


Figure 35 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #1 Crosstalk

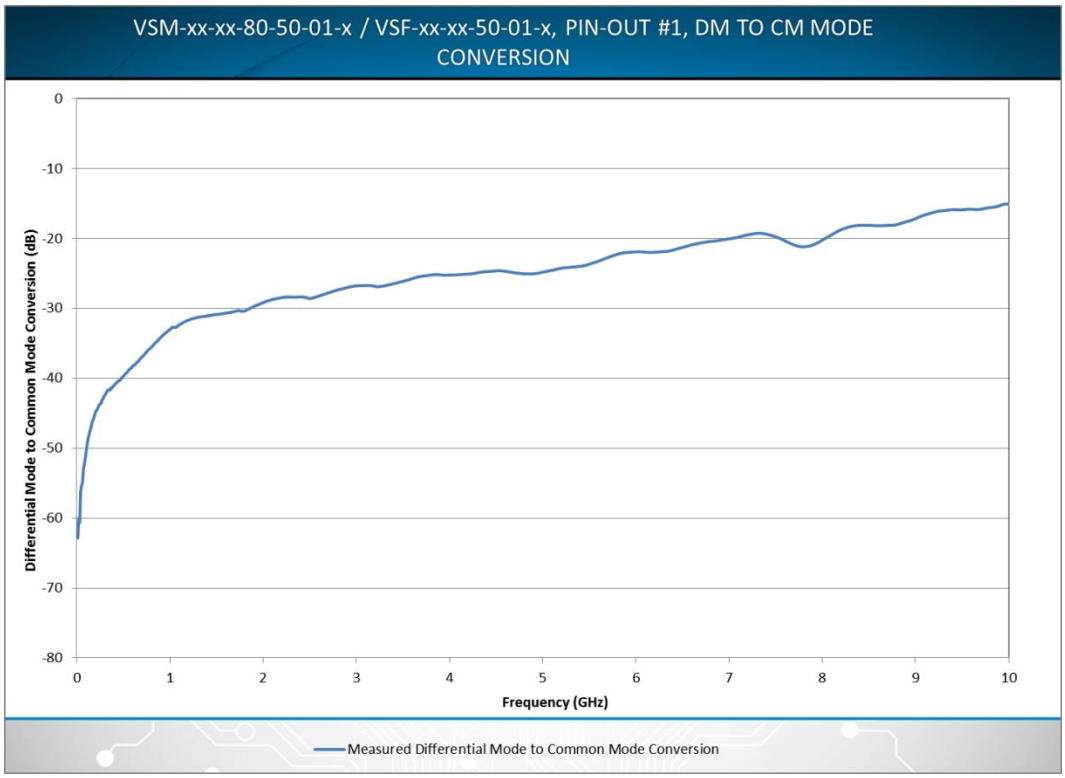


Figure 36 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #1 Mode Conversion

6.1.2 Time Domain Impedance Summary

VSM-xx-xx-80-50-01-x / VSF-xx-xx-50-01-x, Option#1 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 35ps	122.4	97.0
Signal Rise Time - 75ps	104.2	82.9
Signal Rise Time - 140ps	97.4	92.6

Table 14 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #1 Impedance Pair B3/B4 Summary

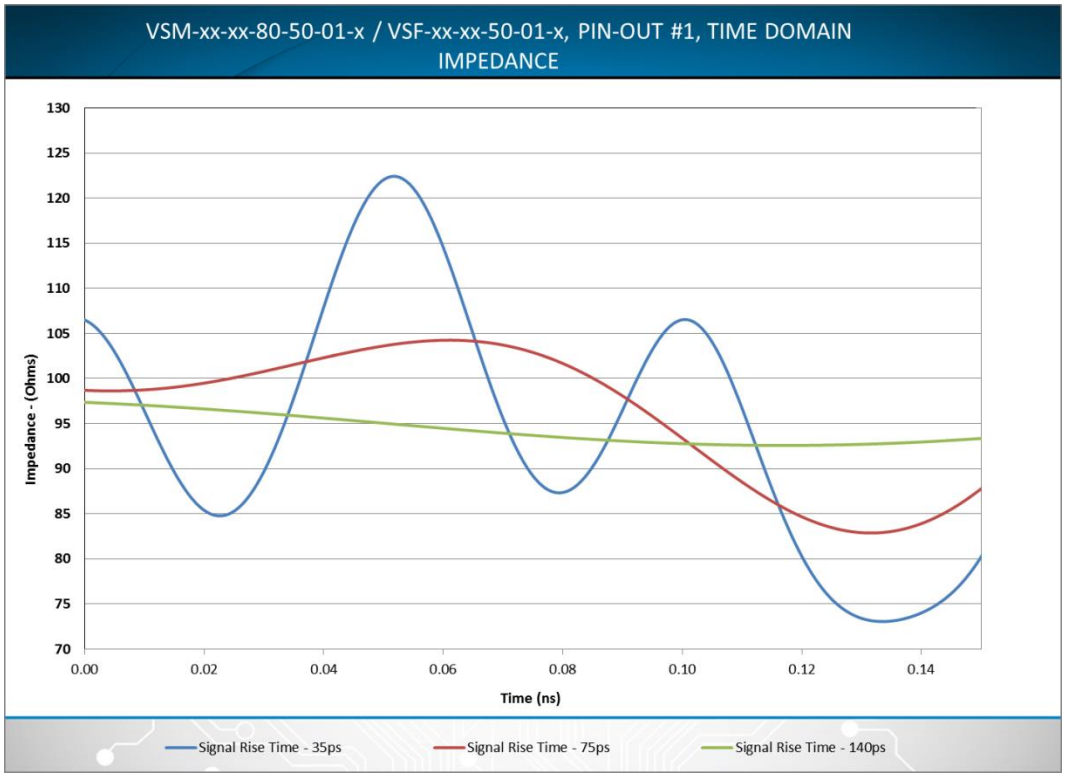


Figure 37 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #1 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

6.2 VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x / Pinout #1

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair C5/C6. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

6.2.1 S-Parameter Summary

Parameter	VSM-04-xx-80-50-01-x / VSRAF-04-xx-50-01-x, Option#1 Typical Mated Performance	
Insertion Loss	-1.3 dB @ 5.0 GHz	-1.9 dB @ 10.0 GHz
Return Loss	-11.7 dB @ 5.0 GHz	-6.6 dB @ 10.0 GHz
Pair to Pair Near-End Crosstalk	-31.8 dB @ 5.0 GHz	-29.7 dB @ 10.0 GHz
Pair to Pair Far-End Crosstalk	-42.3 dB @ 5.0 GHz	-28.6 dB @ 10.0 GHz
Differential Mode to Common Mode Conversion	-22.5 dB @ 5.0 GHz	-17.5 dB @ 10.0 GHz
Propagation Delay	Row D - 84 ps, Row C - 96ps, Row B - 109ps, Row A - 122ps	
Differential Skew	< 2 ps	

Table 15 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #1 S-Parameter Pair C5/C6 Summary

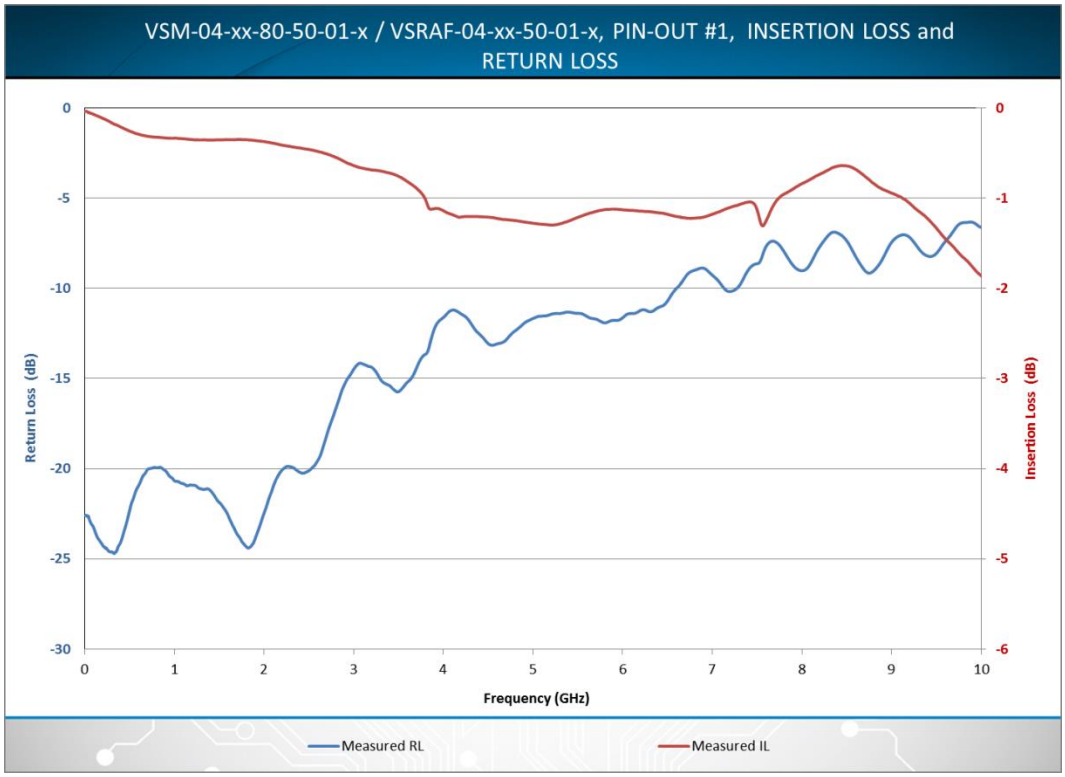


Figure 38 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #1 Insertion Loss/Return Loss

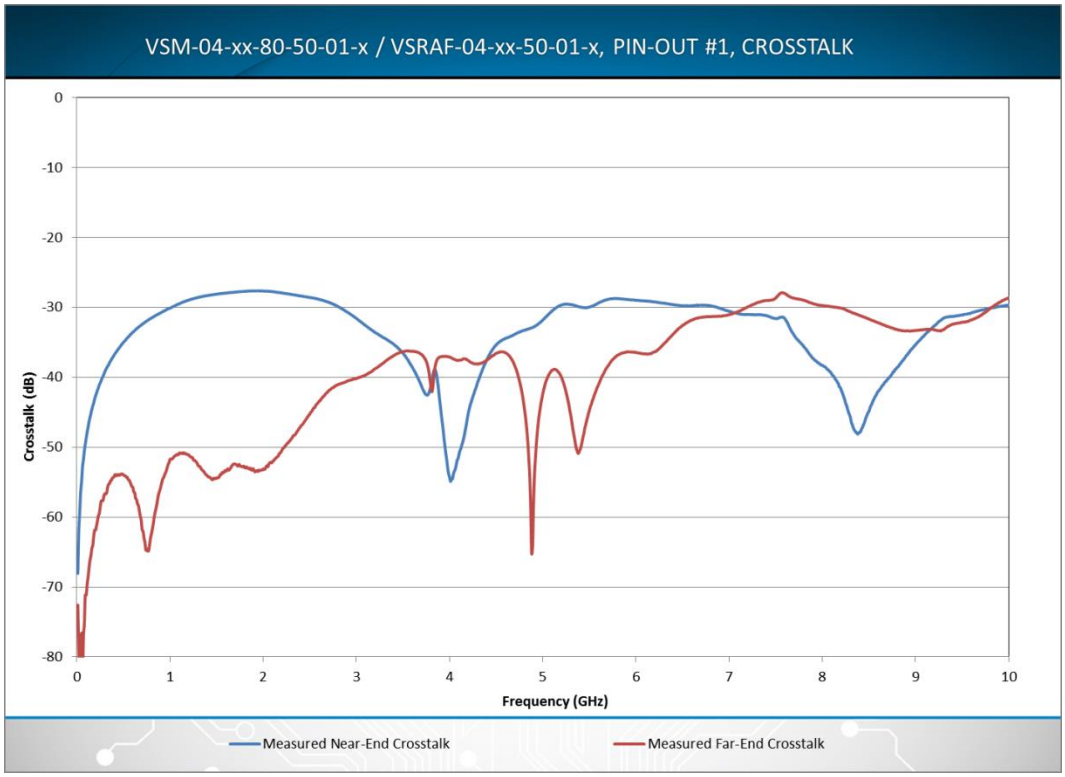


Figure 39 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #1 Crosstalk

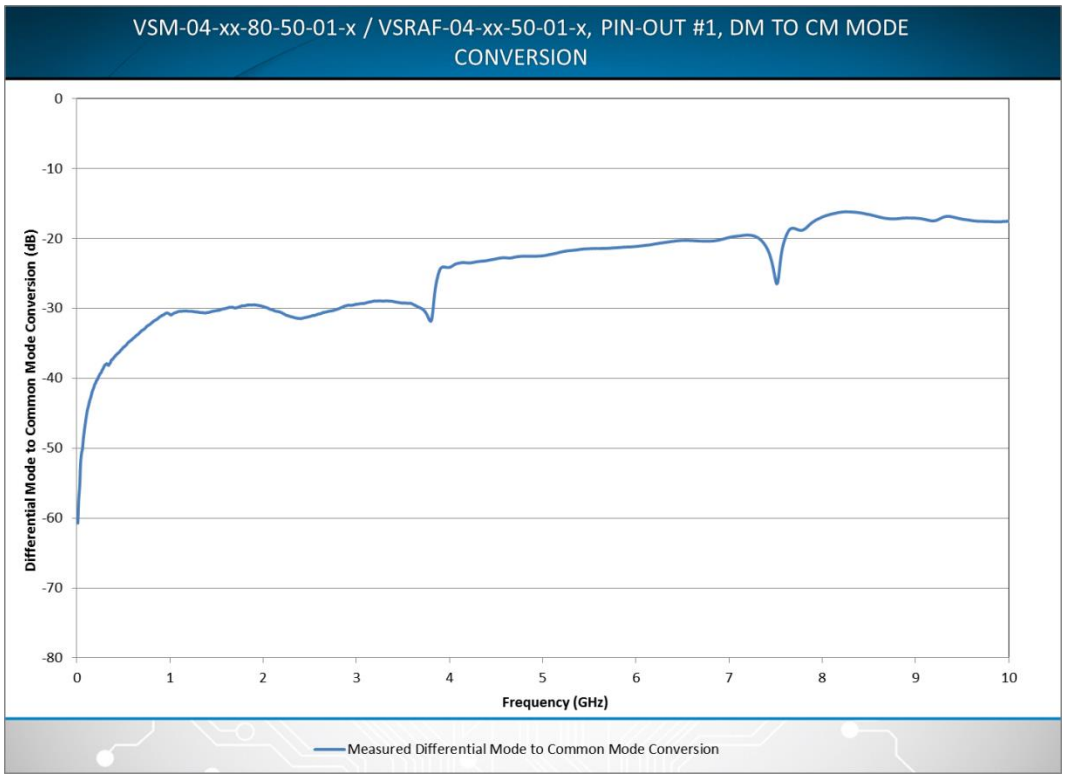


Figure 40 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #1 Mode Conversion

6.2.2 Time Domain Impedance Summary

VSM-04-xx-80-50-01-x / VSRAF-04-xx-50-01-x, Option#1 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 35ps	127.9	76.0
Signal Rise Time - 75ps	123.0	88.1
Signal Rise Time - 140ps	110.4	96.6

Table 16 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #1 Impedance Pair C4/C5 Summary

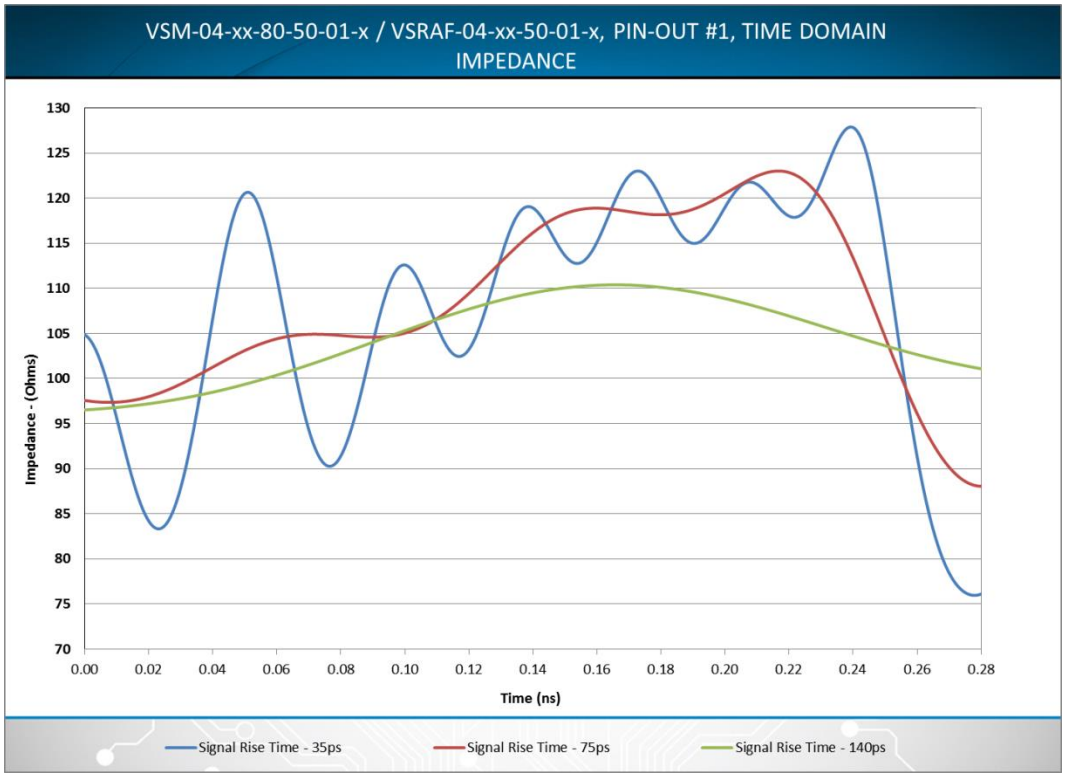


Figure 41 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #1 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

6.3 VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x / Pinout #1

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair B3/B4. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

6.3.1 S-Parameter Summary

Parameter	VSRAM-04-xx-50-01-x / VSRAF-04-xx-50-01-x, Option#1 Typical Mated Performance	
Insertion Loss	-1.6 dB @ 5.0 GHz	-2.1 dB @ 10.0 GHz
Return Loss	-11.0 dB @ 5.0 GHz	-7.5 dB @ 10.0 GHz
Pair to Pair Near-End Crosstalk	-57.5 dB @ 5.0 GHz	-30.4 dB @ 10.0 GHz
Pair to Pair Far-End Crosstalk	-30.1 dB @ 5.0 GHz	-26.8 dB @ 10.0 GHz
Differential Mode to Common Mode Conversion	-38.4 dB @ 5.0 GHz	-28.6 dB @ 10.0 GHz
Propagation Delay	Row D - 140 ps, Row C - 165ps, Row B - 190ps, Row A - 215ps	
Differential Skew	< 2 ps	

Table 17 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #1 S-Parameter Pair B4/B5 Summary

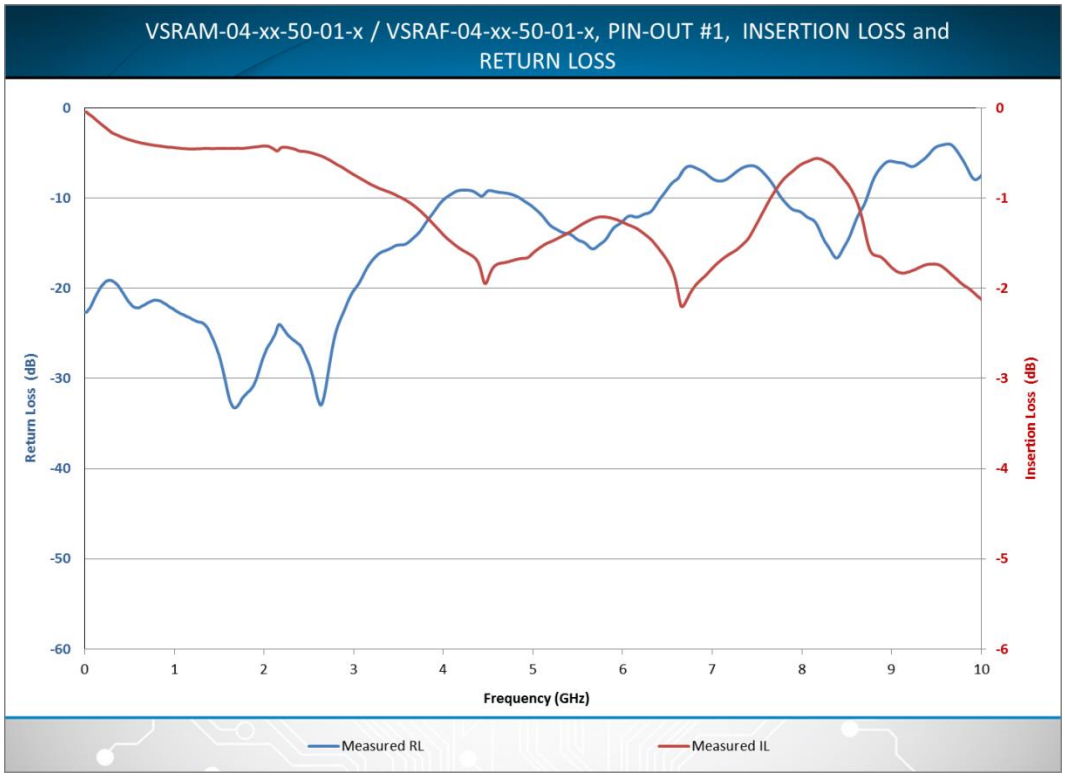


Figure 42 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #1 Insertion Loss/Return Loss

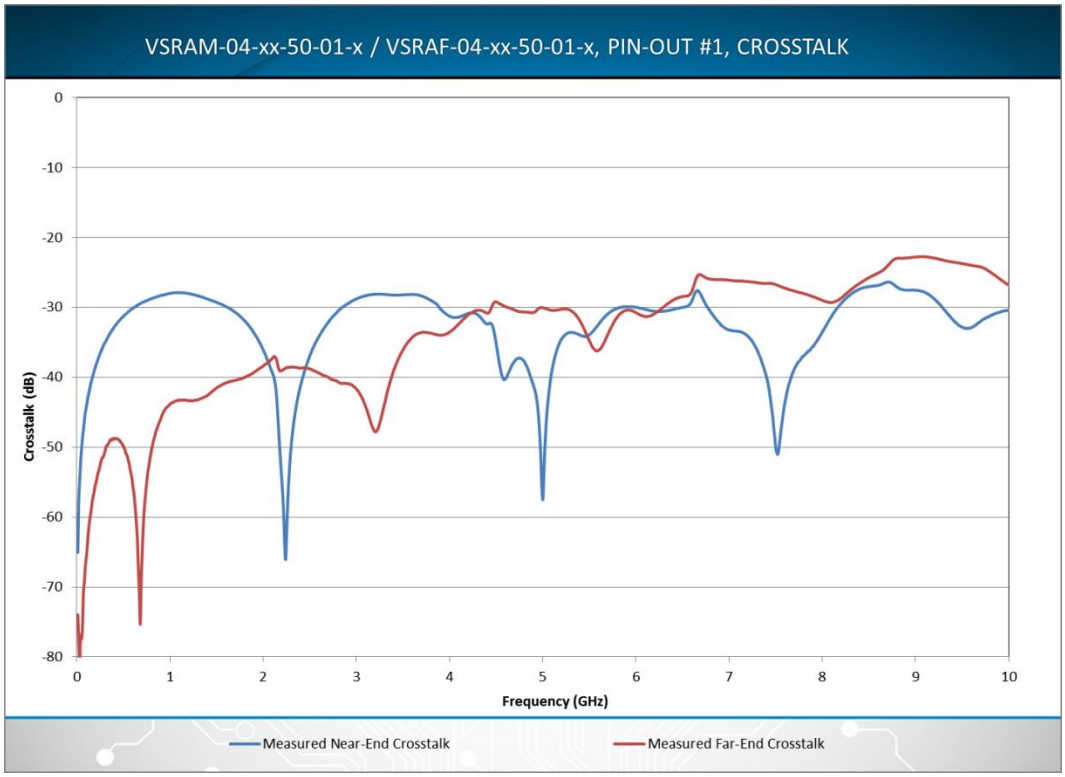


Figure 43 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #1 Crosstalk

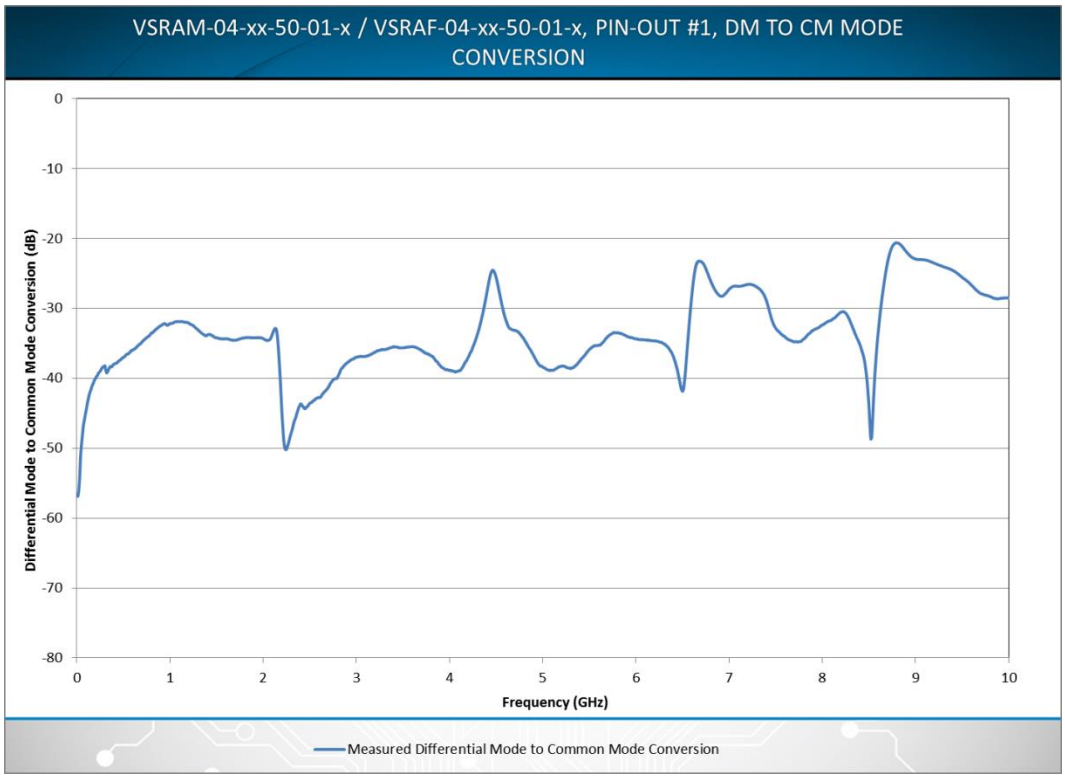


Figure 44 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #1 Mode Conversion

6.3.2 Time Domain Impedance Summary

VSRAM-04-xx-50-01-x / VSRAF-04-xx-50-01-x, Option#1 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 35ps	122.0	70.5
Signal Rise Time - 75ps	114.8	83.8
Signal Rise Time - 140ps	109.5	98.6

Table 18 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #1 Impedance Pair B4/B5 Summary

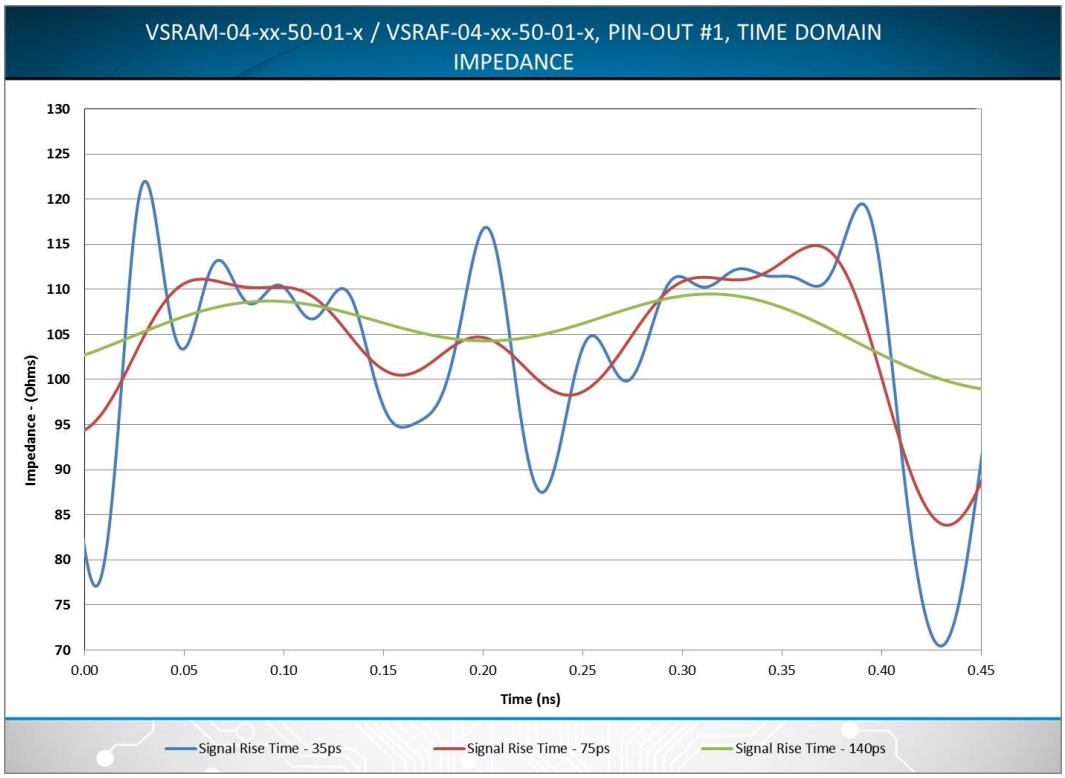


Figure 45 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #1 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

7 Measured SI Performance - Pin-Out Option# 4

7.1 VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x / Pinout #4

- Frequency Domain S-Parameter Summary for pin-out option#2 differential pair B4/B5. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

7.1.1 S-Parameter Summary

Parameter	VSM-xx-xx-80-50-01-x / VSF-xx-xx-50-01-x, Option#4 Typical Mated Performance	
Insertion Loss	-0.3 dB @ 2.5 GHz	-0.6 dB @ 5.0 GHz
Return Loss	-38.3 dB @ 2.5 GHz	-11.0 dB @ 5.0 GHz
Pair to Pair Near-End Crosstalk	-34.3 dB @ 2.5 GHz	-26.1 dB @ 5.0 GHz
Pair to Pair Far-End Crosstalk	-36.9 dB @ 2.5 GHz	-27.6 dB @ 5.0 GHz
Differentail Mode to Common Mode Conversion	-32.5 dB @ 2.5 GHz	-27.5 dB @ 5.0 GHz
Propagation Delay	75 ps	
Differential Skew	< 2 ps	

Table 19 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #4 S-Parameter Pair B4/B5 Summary

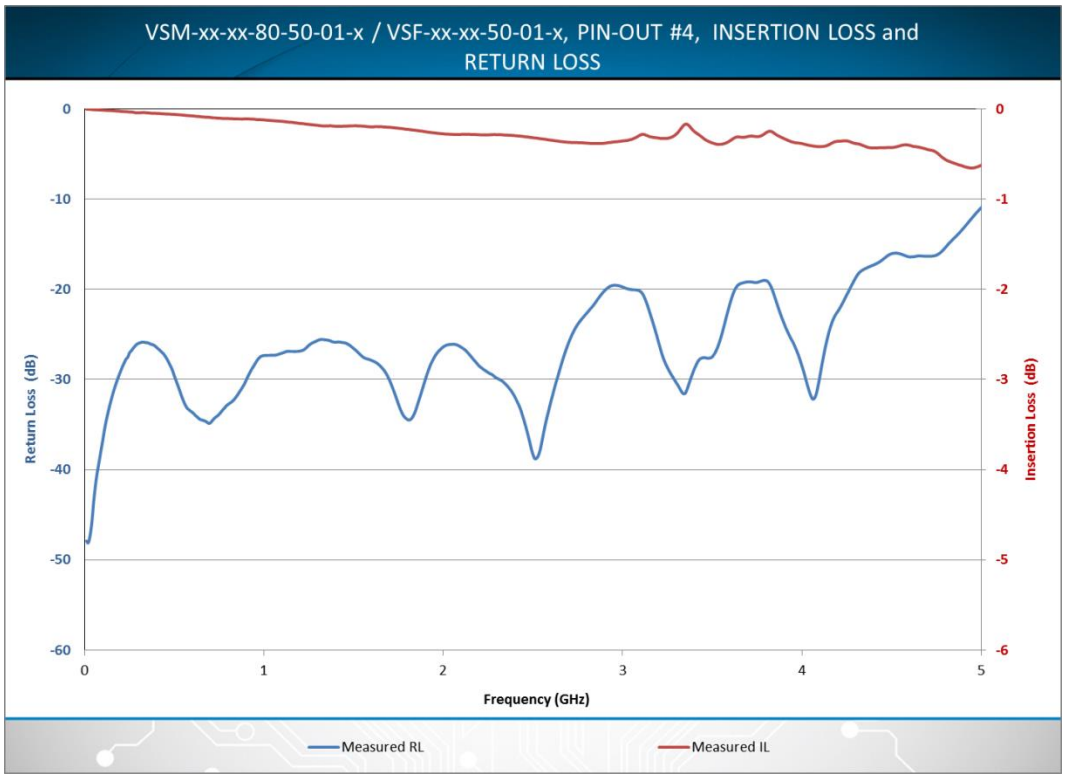


Figure 46 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #4 Insertion Loss/Return Loss

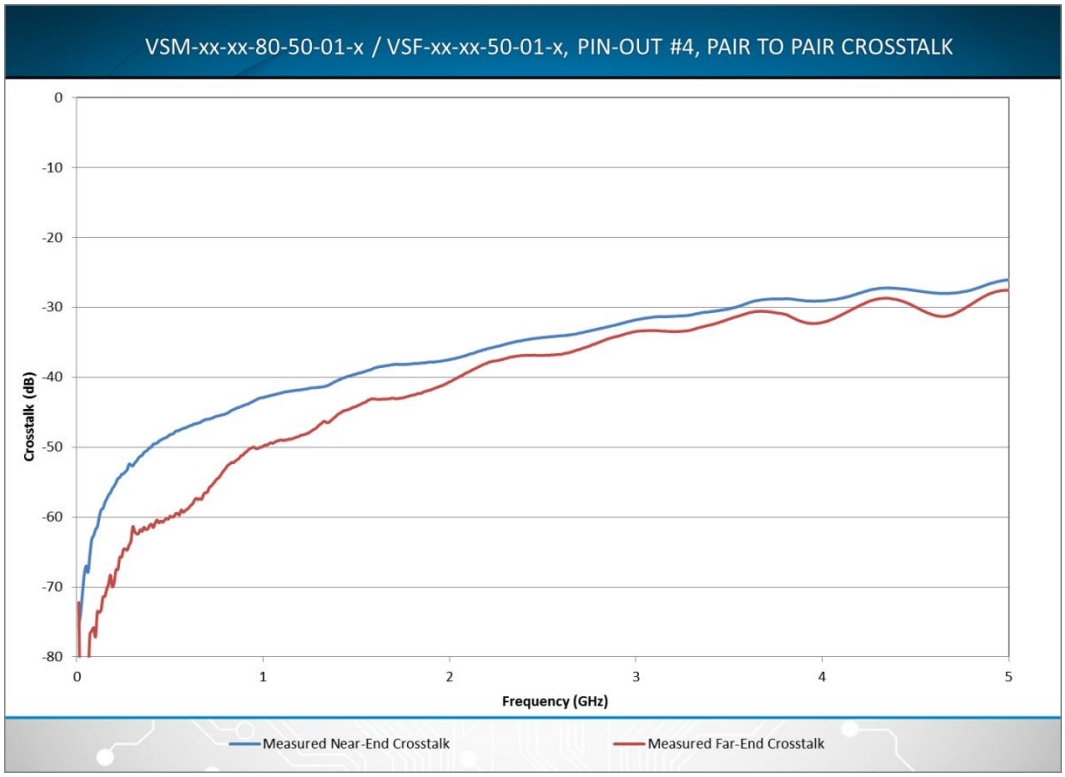


Figure 47 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #4 Crosstalk

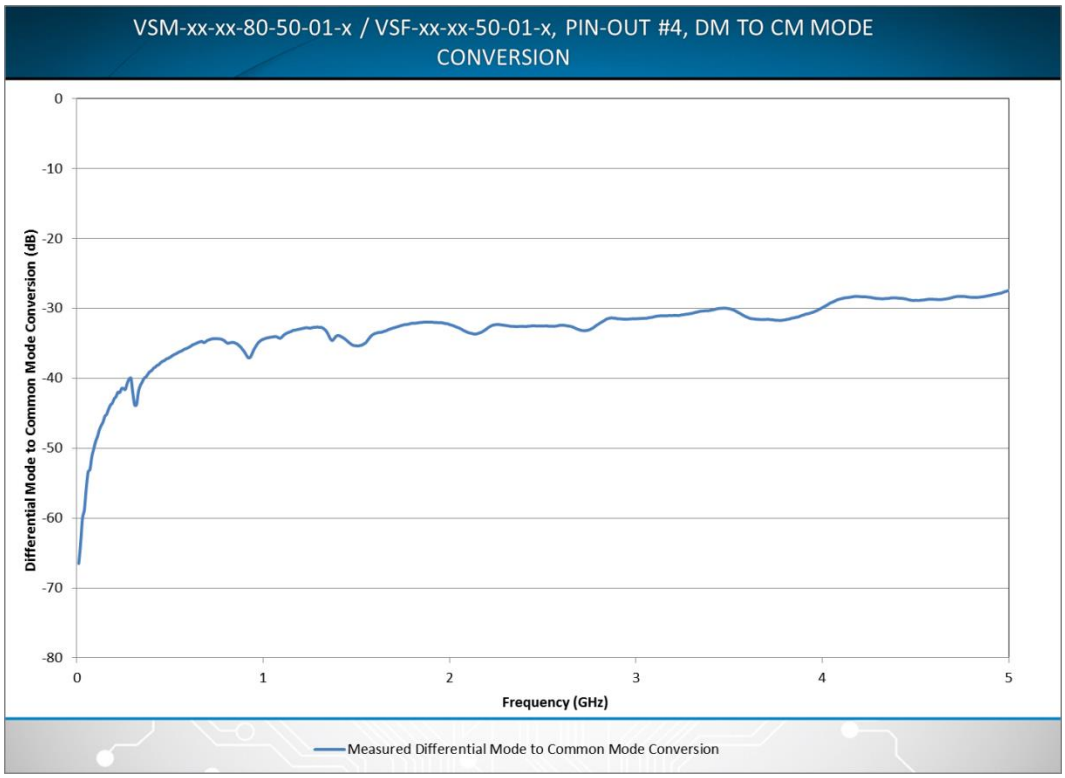


Figure 48 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #4 Mode Conversion

7.1.2 Time Domain Impedance Summary

- Frequency Domain S-Parameter Summary for pin-out option#2 differential pair B4/B5. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance.

VSM-xx-xx-80-50-01-x / VSF-xx-xx-50-01-x, Option#4 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 140ps	102.3	97.4

Table 20 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #4 Impedance Pair B4/B5 Summary

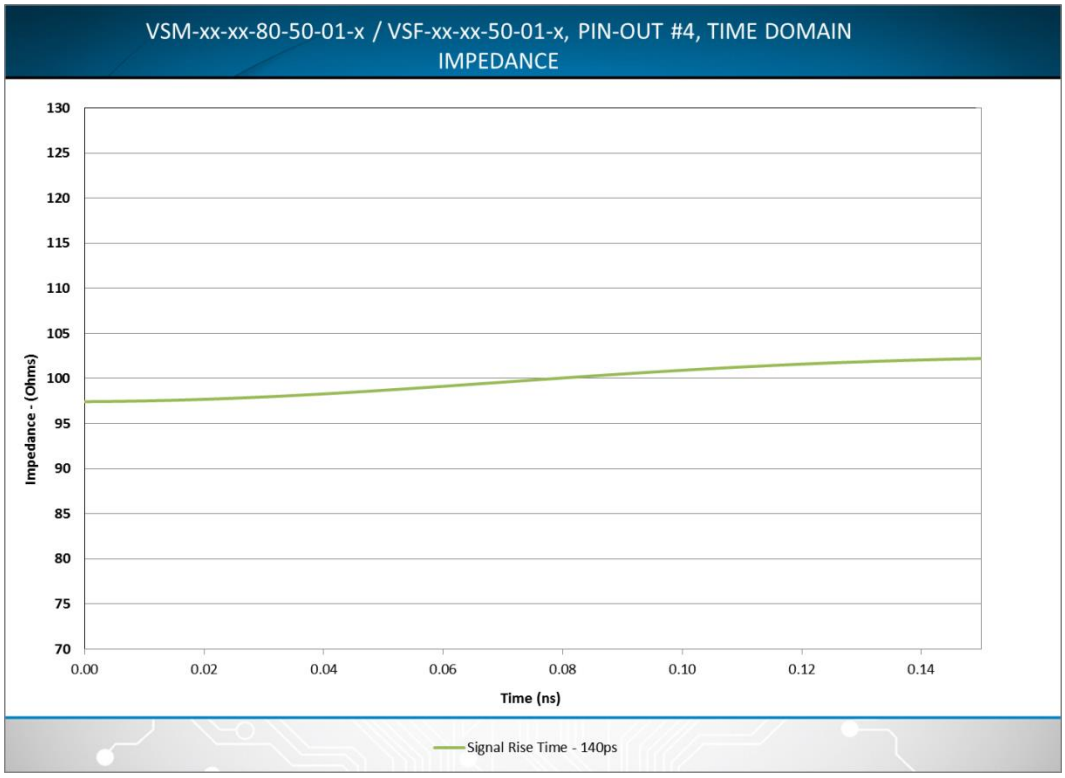


Figure 49 - VSM-xx-xx-080-50-01-x / VSF-xx-xx-50-01-x - #4 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

7.2 VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x / Pinout #4

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair B4/B5. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. . The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

7.2.1 S-Parameter Summary

Parameter	VSM-xx-xx-80-50-01-x / VSRAF-04-xx-50-01-x, Option#4 Typical Mated Performance	
Insertion Loss	-0.7 dB @ 2.5 GHz	-0.9 dB @ 5.0 GHz
Return Loss	-14.0 dB @ 2.5 GHz	-14.8 dB @ 5.0 GHz
Pair to Pair Near-End Crosstalk	-30.1 dB @ 2.5 GHz	-32.1 dB @ 5.0 GHz
Pair to Pair Far-End Crosstalk	-41.3 dB @ 2.5 GHz	-34.9 dB @ 5.0 GHz
Differentail Mode to Common Mode Conversion	-33.2 dB @ 2.5 GHz	-27.5 dB @ 5.0 GHz
Propagation Delay	RowD- 83 ps, RowC- 95ps, RowB- 110ps, RowA - 123ps	
Differential Skew	< 2 ps	

Table 21 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #4 S-Parameter Pair C5/C6 Summary

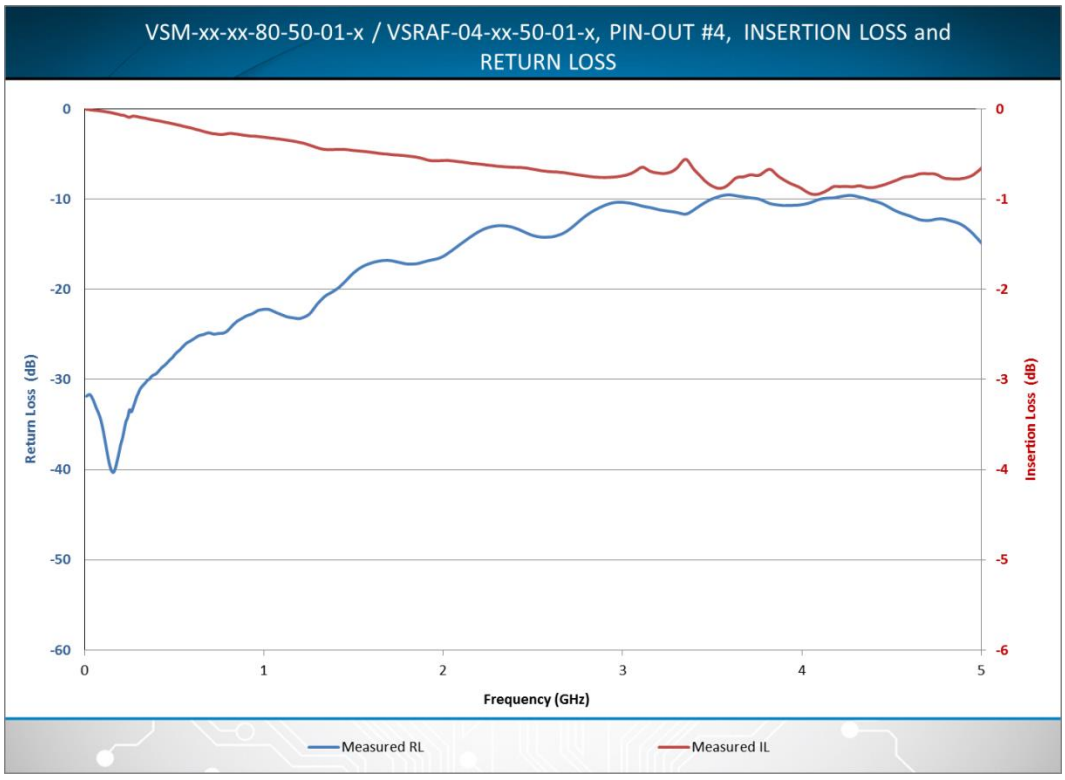


Figure 50 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #4 Insertion Loss/Return Loss

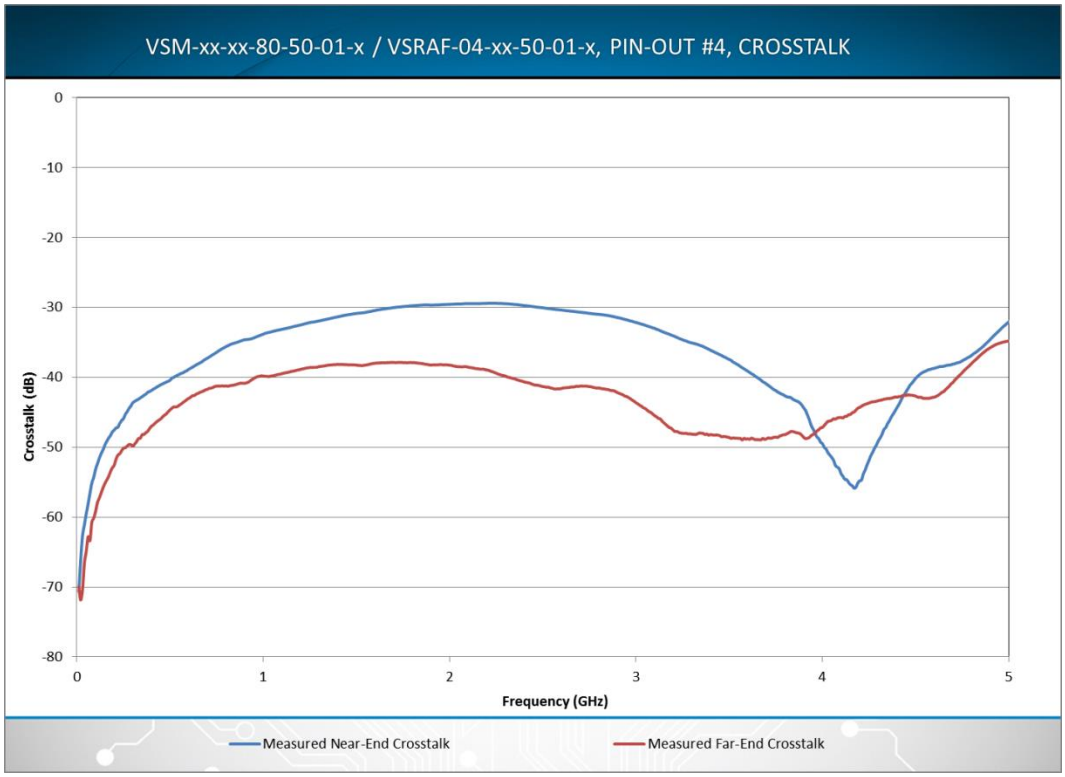


Figure 51 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #4 Crosstalk

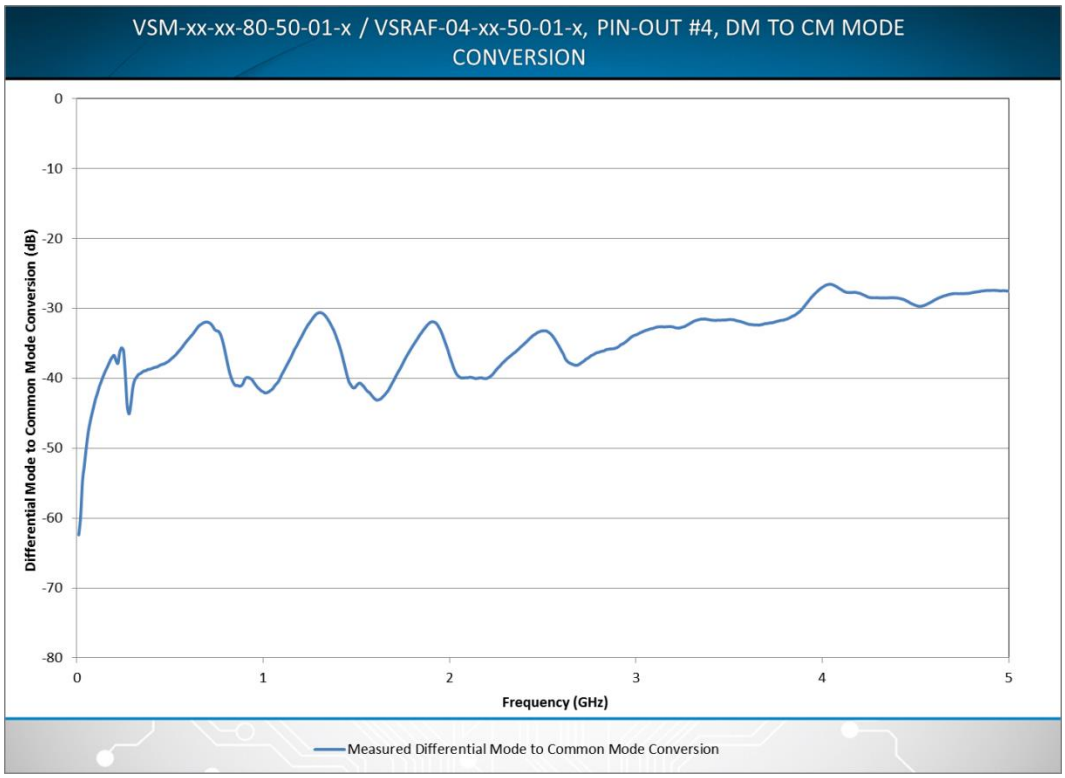


Figure 52 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #4 Mode Conversion

7.2.2 Time Domain Impedance Summary

VSM-xx-xx-80-50-01-x / VSRAF-04-xx-50-01-x, Option#4 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 140ps	118.0	96.6

Table 22 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #4 Impedance Pair C4/C5 Summary

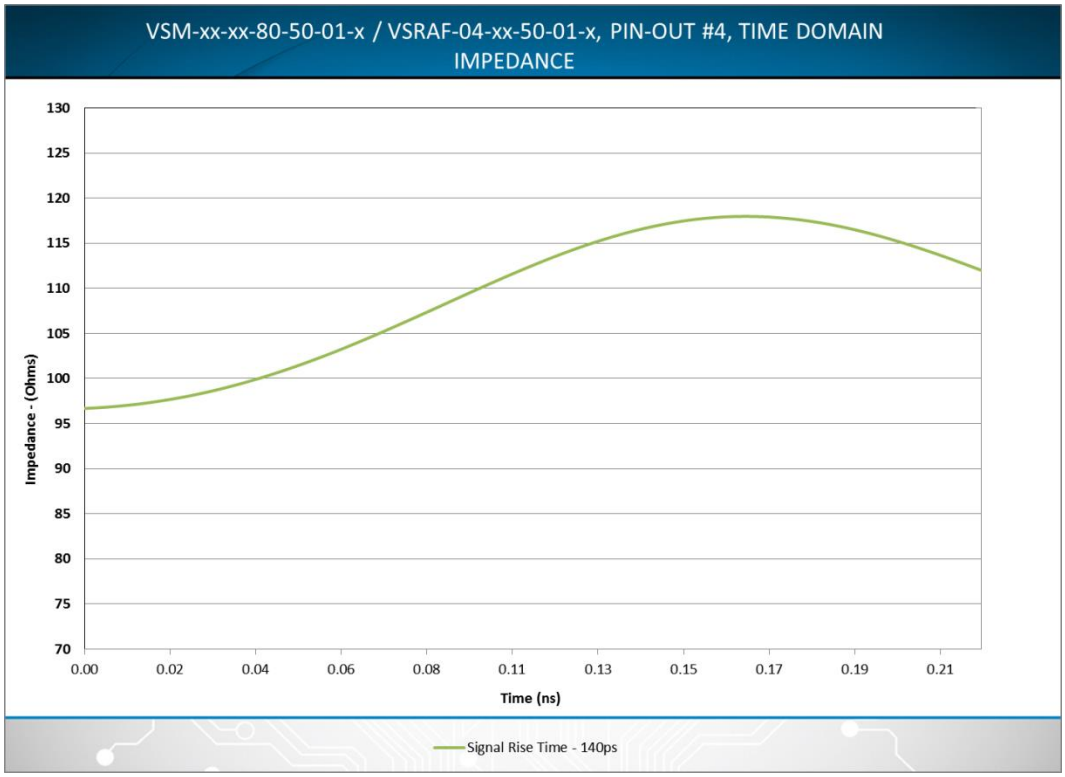


Figure 53 - VSM-xx-xx-080-50-01-x / VSRAF-xx-xx-50-01-x - #4 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

7.3 VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x / Pinout #4

- Frequency Domain S-Parameter Summary for pin-out option#3 differential pair B4/B5. Differential pairs not in this equivalent physical position will have slightly varying bandwidth performance. Measurements include the PCB thru hole used to solder the verSI PIH pins to the PCB. The test fixture traces and SMA launch connectors have been de-embedded out from the measurement. Future revision to the measurement fixture may improve the fixture de-embedding accuracy.

7.3.1 S-Parameter Summary

Parameter	VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x, Option#4 Typical Mated Performance	
Insertion Loss	-0.2 dB @ 2.5 GHz	-1.7 dB @ 5.0 GHz
Return Loss	-18.1 dB @ 2.5 GHz	-4.6 dB @ 5.0 GHz
Pair to Pair Near-End Crosstalk	-41.2 dB @ 2.5 GHz	-40.3 dB @ 5.0 GHz
Pair to Pair Far-End Crosstalk	-47.4 dB @ 2.5 GHz	-37.4 dB @ 5.0 GHz
Differentail Mode to Common Mode Conversion	-33.2 dB @ 2.5 GHz	-26.0 dB @ 5.0 GHz
Propagation Delay	Row D - 140 ps, Row C - 165ps, Row B - 190ps, Row A - 215ps	
Differential Skew	< 2 ps	

Table 23 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #4 S-Parameter Pair B4/B5 Summary

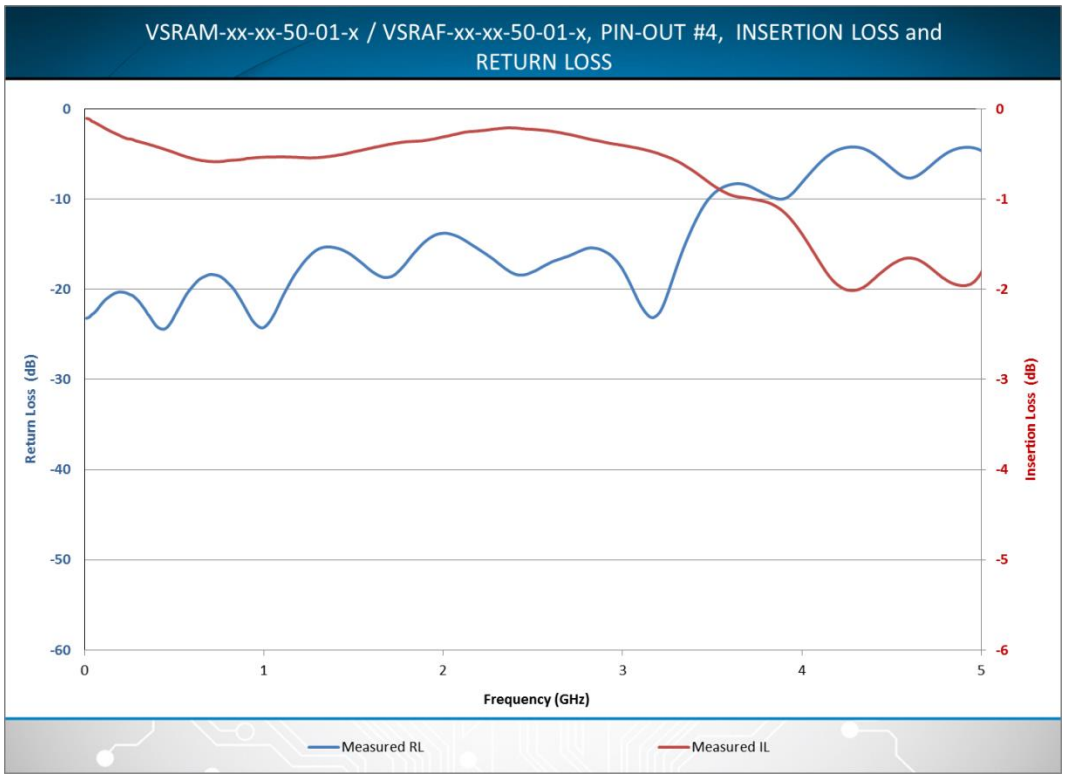


Figure 54 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #4 Insertion Loss/Return Loss

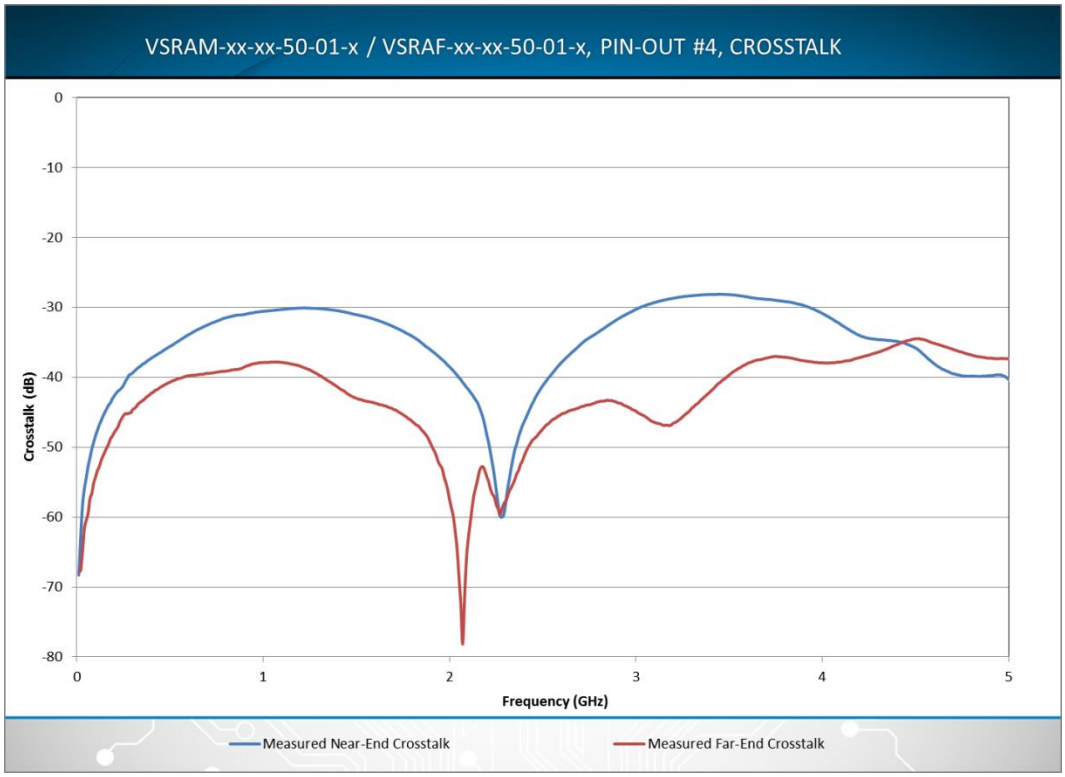


Figure 55 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #4 Crosstalk

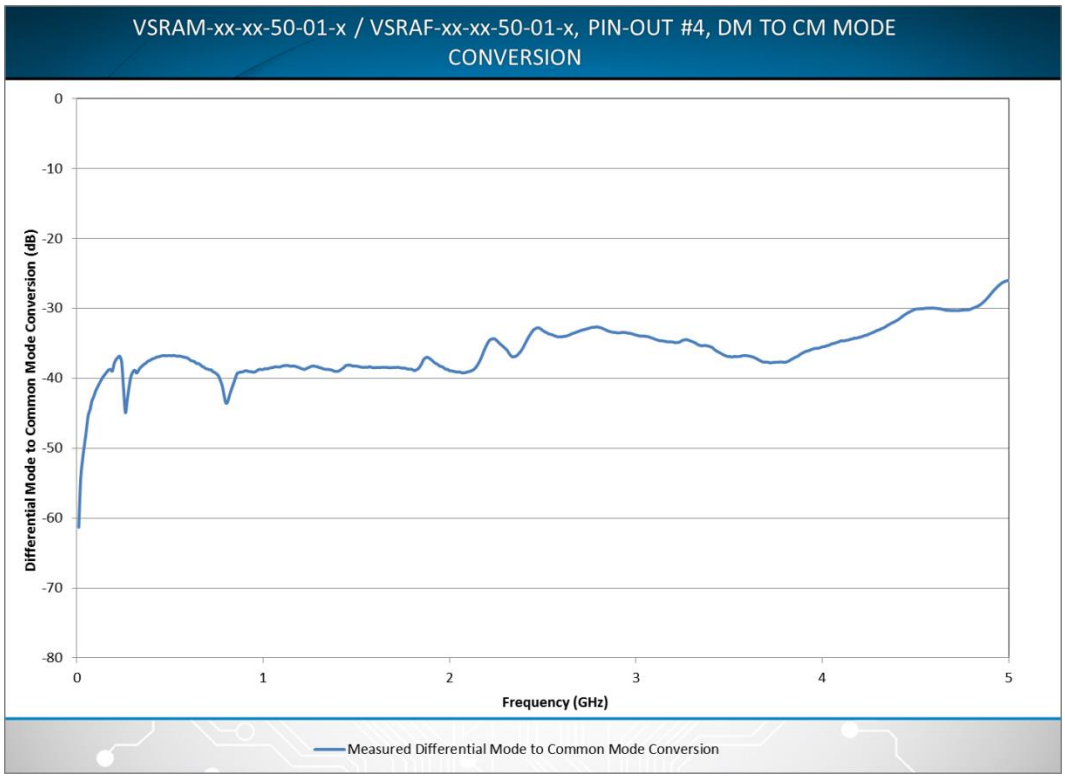


Figure 56 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #4 Mode Conversion

7.3.2 Time Domain Impedance Summary

VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x, Option#4 Typical Mated Impedance		
Impedance (Ohms)	**Maximum**	**Minimum**
Signal Rise Time - 140ps	111.8	89.8

Table 24 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #4 Impedance Pair B4/B5 Summary

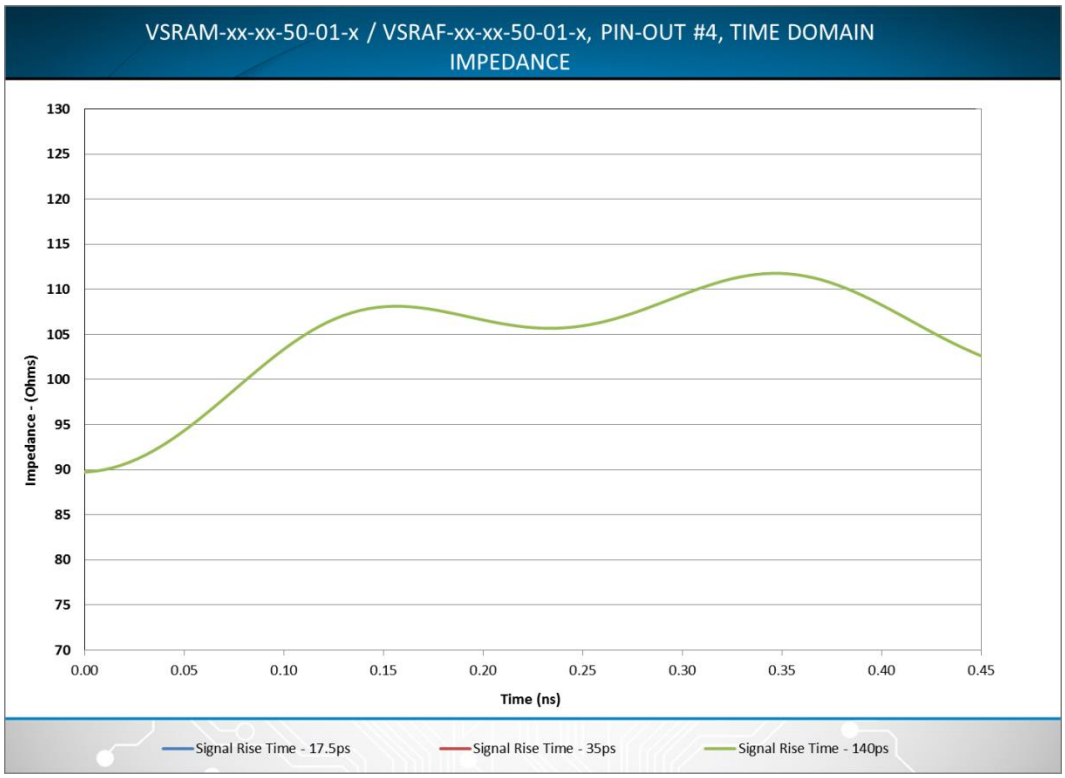


Figure 57 - VSRAM-xx-xx-50-01-x / VSRAF-xx-xx-50-01-x - #4 Time Domain Impedance

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

8 verSI Measured Mated Connector S-Parameter Exports

8.1 S-Parameter Measured Files Available

Due to the very large amount of possible verSI mated combinations and pinouts, not all measurements are available.

See AirBorn Web site for available verSI Series measurements

See AirBorn Sales / Marketing to request different mated measurement combinations

8.1.1 S-Parameter File Name Definition

EX: OPT#1 VSM-xx-xx-80-50-01_VSF-xx-xx-50-01_B4B5_15GHz.s4p

Pinout	Logical Port1 (1, 3)	Logical Port 2 (2, 4)	Pin Location	Data Bandwidth
OPT#1	VSM-xx-xx-80-50-01 (Male)	VSF-xx-xx-50-01 (Female)	B4, B5	15GHz

See **Section 3, verSI Series Open Pin Field Pin-Out Options** for more detail on Pinout and Pin Location

See **Figure 58 - S-Parameter Export 4 Port** Configuration for example S-Parameter Configuration

See **Figure 59 - DUT Port Topology** for logical port definition

8.1.2 S-Parameter File Port Definitions

Logical Port #1 is made up of single ended port #1 and #3
Logical Port #2 is made up of single ended port #2 and #4

Logical Port #1 is always terminated to the male verSI connector
Logical Port #2 is always terminated to the female verSI connector

```
!$DUT_CFG_DESC: Default 4-Port Configuration
!$NUMBER_PORTS: 4
!$DIFF_PORT_MAP: 1|2P|2|2P|0|UC|0|UC|
!$PORT_MAP: 1|1|<<<<<<|2|2|>>>>>>|3|3|<<<<<<|4|4|>>>>>>|
!Date: Monday, May 21, 2018, 09:56:02
!S4P File: Measurements: <S11,S12,S13,S14>,
!<S21,S22,S23,S24>,
!<S31,S32,S33,S34>,
!<S41,S42,S43,S44>:
```

Figure 58 - S-Parameter Export 4 Port Configuration

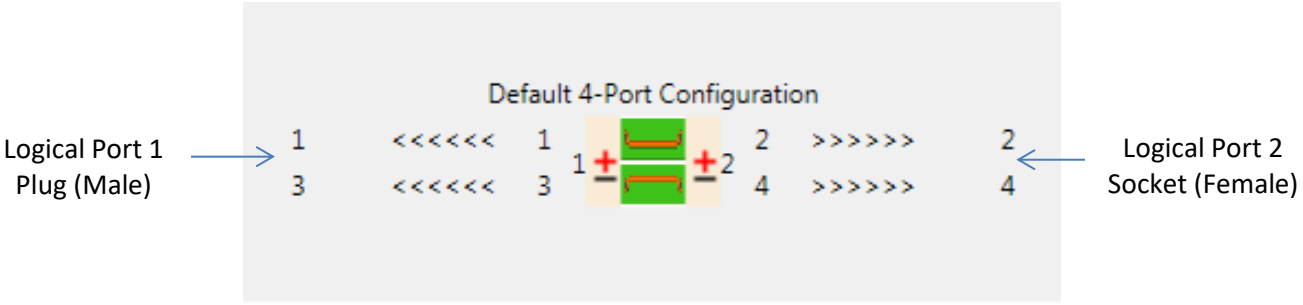


Figure 59 - DUT Port Topology

9 verSI Simulated Mated Connector S-Parameter Exports

9.1 S-Parameter Simulation 3D Model Sample

- All simulations include paste-in-hole (PIH) PCB terminations.
- All simulations include PCB with plated thru holes and back drilling were possible.
- All unused pins in all simulations are grounded.
- Signal traces in simulations have been de-embedded.
- Simulations include pair to pair performance variation caused by pair location and plated thru hole (PTH) depth used in the artwork breakout.

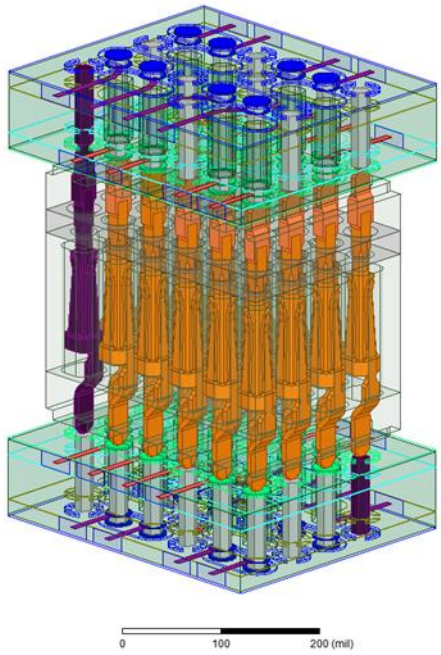


Figure 60 - Sample Mated VerSI Model

NOTE: Any variation to this simulation will alter performance

NOTE: Simulations are one case of a nominal best case scenario

NOTE: Always plan for channel performance margin in a design to take into account manufacturing variability.

NOTE: Improper design of the connector PCB breakout can reduce mated connector performance

9.2 S-Parameter Simulation Port Definitions

- See Section 3 on page 10 for pin out Option details
- Ex: P_D2 - Plug side, Row D, Pin 2
- Ex: S_C5 - Socket side, Row C, Pin 5
- Any missing pins in the port definitions are grounded in the simulation
- Ex: VerSI Pin S_A1 and P_A1 are not listed but are grounded in the simulation

```
! Terminal data exported
! Port[1] = S_A2
! Port[2] = S_A3
! Port[3] = S_A5
! Port[4] = S_A6
! Port[5] = S_B1
! Port[6] = S_B2
! Port[7] = S_B4
! Port[8] = S_B5
! Port[9] = S_C2
! Port[10] = S_C3
! Port[11] = S_C5
! Port[12] = S_C6
! Port[13] = S_D1
! Port[14] = S_D2
! Port[15] = S_D4
! Port[16] = S_D5
! Port[17] = P_A2
! Port[18] = P_A3
! Port[19] = P_A5
! Port[20] = P_A6
! Port[21] = P_B1
! Port[22] = P_B2
! Port[23] = P_B4
! Port[24] = P_B5
! Port[25] = P_C2
! Port[26] = P_C3
! Port[27] = P_C4
! Port[28] = P_C5
! Port[29] = P_D1
! Port[30] = P_D2
! Port[31] = P_D4
! Port[32] = P_D5
```

Table 25 - Sample Simulation Port Definitions

9.2.1 S-Parameter Sample Simulation File Name Definition

- EX: VSM-04-06-080-xx-01, VSF-04-06-xx-01, Option #1.sXXp

Logical Port1 (P_XX)	Logical Port 2 (S_XX)	Pinout	Ports Simulated
VSM-x4-x6-80-xx-01 (Male)	VSF-xx-xx-50-01 (Female)	Option #1	.sXXp

See **Section 3, verSI Series Open Pin Field Pin-Out Options** for more detail on Pinout and Pin Location

9.3 S-Parameter Simulation Correlation to Measured Data

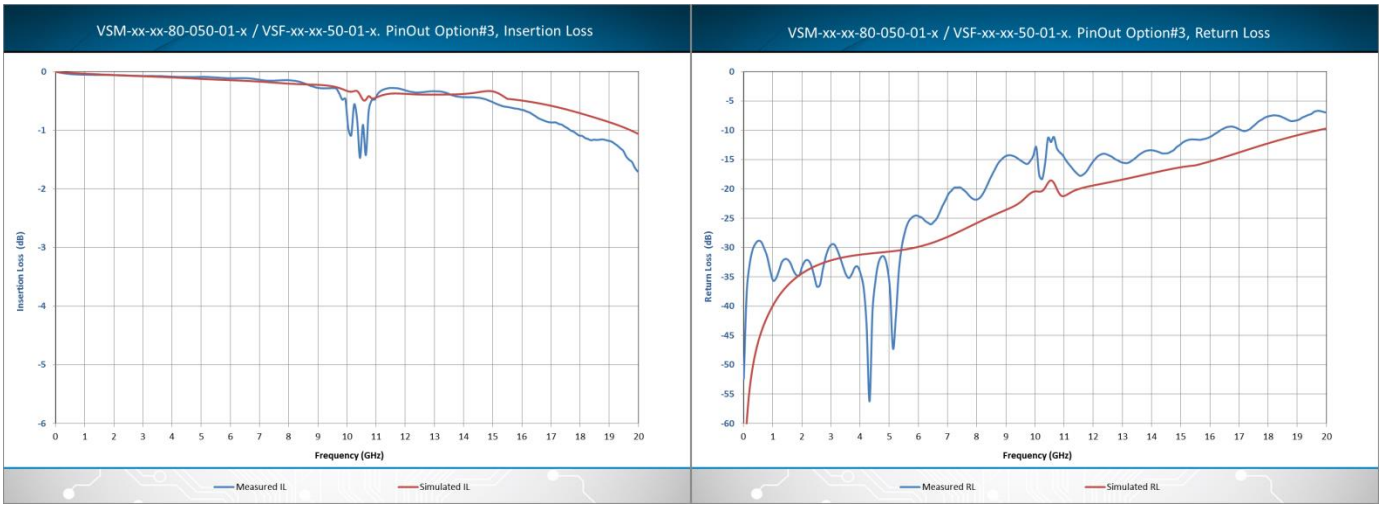


Figure 61 – Option #3 Sample Simulated to Measured Correlation

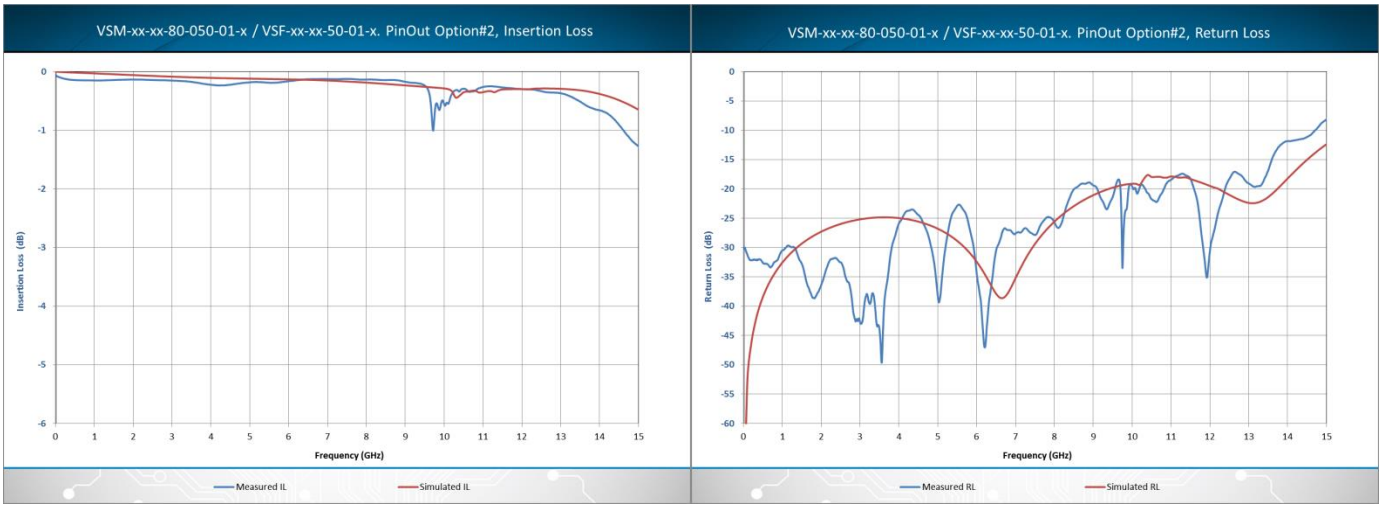


Figure 62 – Option #2 Sample Simulated to Measured Correlation

NOTE: Future revisions to test fixtures and fixture de-embedding artifacts should further improve correlation

9.4 S-Parameter Simulations Available

Due to the very large amount of possible verSI mated combinations and pinouts, not all simulations are available.

See AirBorn Web site for available verSI Series simulations
https://www.airborn.com/products/connectors/versi/electrical-models/

See AirBorn Sales / Marketing to request different mated simulation combinations

10 verSI Connector PCB Layout and Breakout Recommendations

10.1 Connector Footprint

See AirBorn Document: verSI SERIES PRODUCT GUIDE, ESL5001 for details

10.2 PCB Material parameters that will influence high speed connector PCB breakout regain performance

- Dielectric Constant (Dk) - Main contributor to capacitive coupling which contributes to impedance
- Dissipation Factor (Df) – Large contributor to insertion loss. High Speeds need lower Df values
- Typical “Lower Speed” (< 2.5GHz bandwidth), FR-4 material variety
- Typical “High Speed” (< 15GHz bandwidth), Nelco 4000-13EP, Nelco 4000-13EP SI or Megtron6

10.3 Plated Thru Hole Bandwidth Limitation - Vias / Stubs / Back-drilling

- Drill thru vias are the least costly but can leave a long capacitive stub below a signal trace
- Long via stubs or pin stubs degrade signal performance at high speeds
- Back drilling the via stub adds cost but is often used in high speed designs
- After back drilling, stubs length can be as short as 10mil
- Long stub length on both sides of the verSI mated connector may further reduce the usable bandwidth

Signal Degradation Start Frequency (GHz)			
	Printed Circuit Board Material		
Stub Length	**FR-4**	**N4000-13**	**RO3003**
10mil	18.0	24.2	31.0
20mil	9.0	12.1	15.5
30mil	6.0	8.0	10.4
60mil	3.0	4.0	5.0
90mil	2.0	2.7	3.4
120mil	1.5	2.0	2.7
150mil	1.2	1.5	2.1
180mil	1.0	1.4	1.7

- Note: Higher bandwidths may be possible but at addition insertion loss due to the long stub length

Table 26 - When Stub Length Starts Affecting Signal Quality

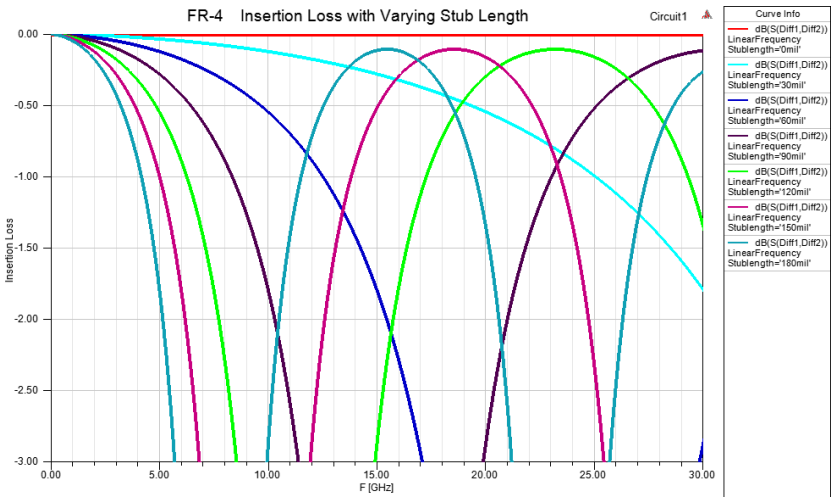


Figure 63 - FR-4 Stub Length Insertion Loss

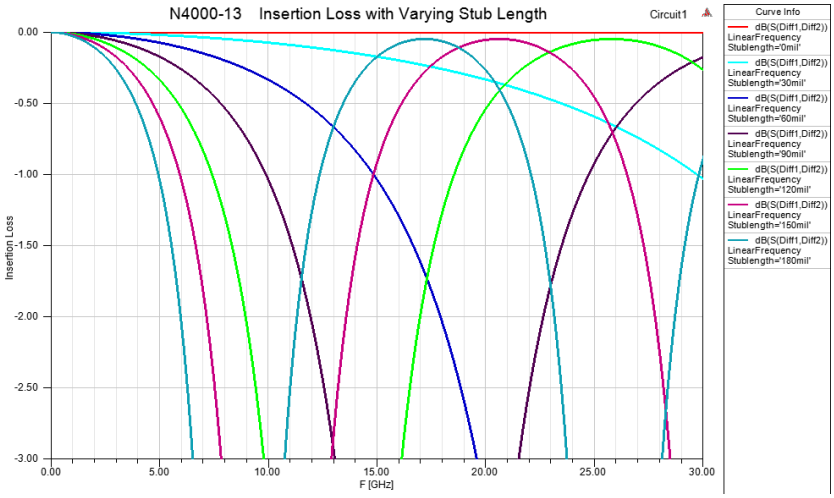


Figure 64 - N4000-13 Stub Length Insertion Loss

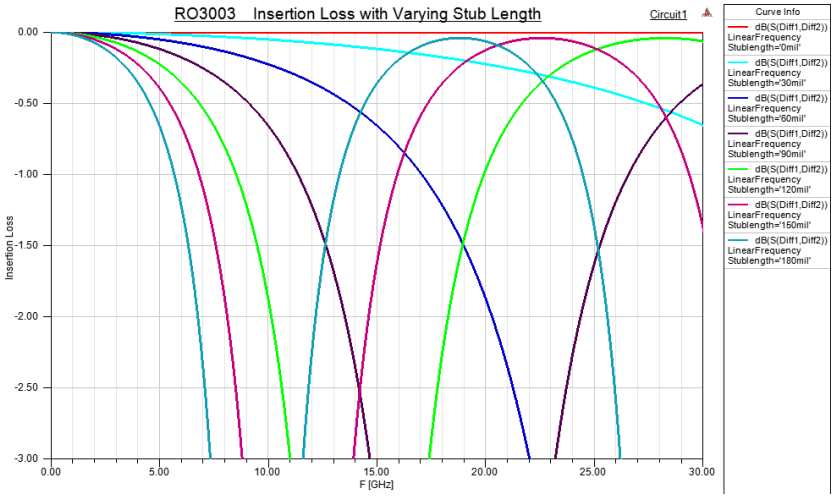


Figure 65 - RO3003 Stub length Insertion Loss

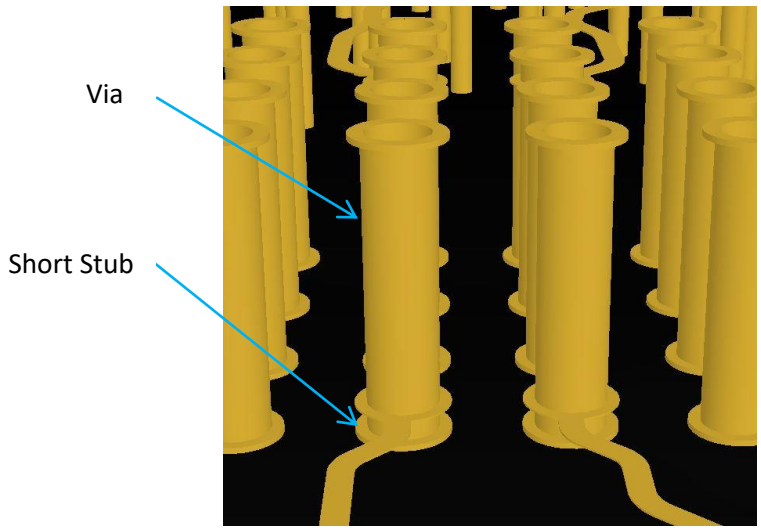


Figure 66 - Short Via Stub

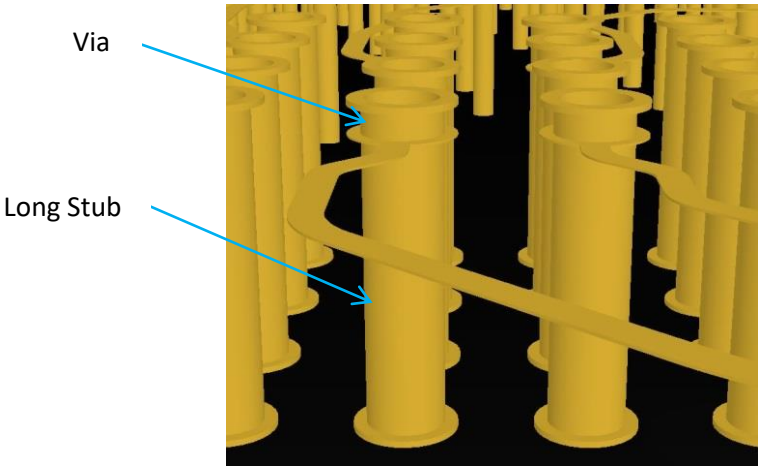


Figure 67 - Long Via Stub

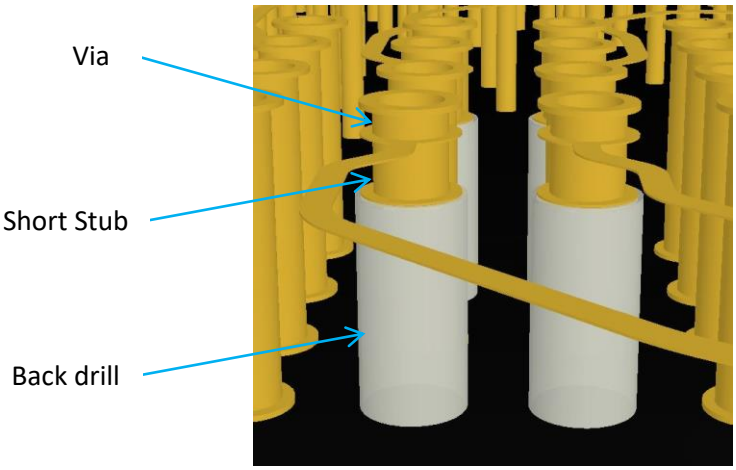


Figure 68 - Back drilled Via Stub

10.4 Anti-pad Diameter Factors

- Larger Diameter advantage
  - reduced via capacitive coupling, higher impedance, increase voltage breakdown
- Larger Diameter disadvantage
  - reduced routing widths, longer trace mismatch under anti-pad

- Smaller Diameter advantage
  - reduce EMI and crosstalk to adjacent pairs, improved signal trace reference to ground
- Smaller Diameter disadvantage
  - reduced routing widths, longer trace mismatch under anti-pad
  - non-functional via pads can be removed for smaller anti-pad diameters

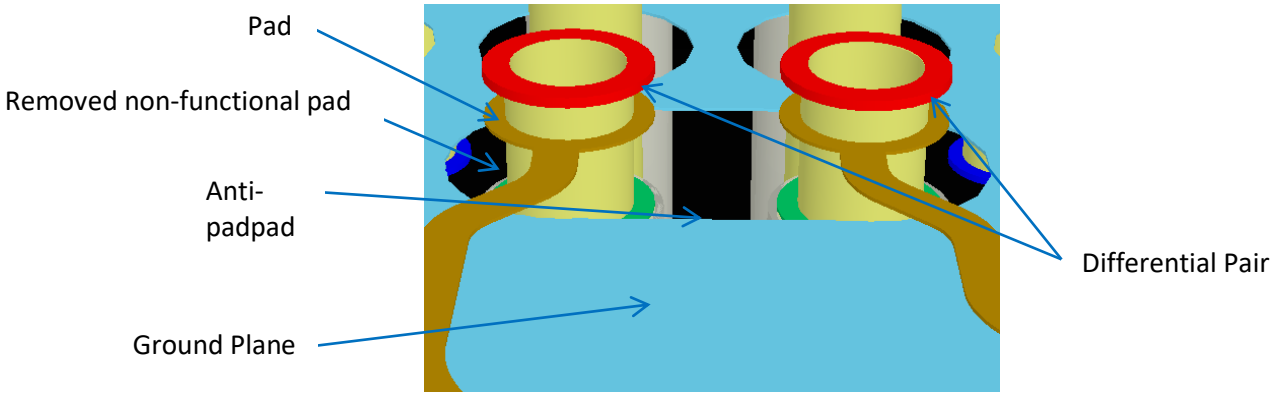


Figure 69 - Anti-pad Description

10.5 Non-Functional Plated Thru Hole Pads and connections

- It is recommended that all unused verSI thru holes are terminated to ground to improve isolation and reduce unwanted high speed signal reflections

10.6 Signal Trace Balance / Return Signal Path

- It is recommended for optimum high speed performance that as many as possible ground return pins are provided around the signal pin
- The ground pins should be symmetrical around differential signal pins to provide a balanced return path within a differential pair
    - An unbalance return path in a differential pair can cause mode conversions leading to intrapair skew issues

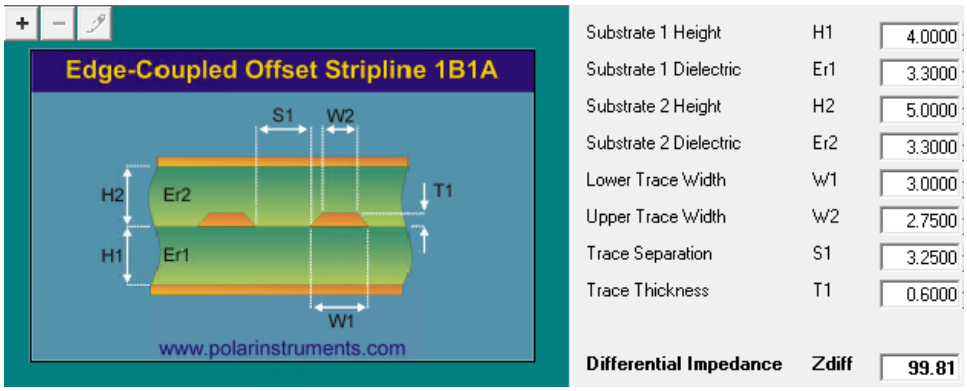
10.7 Connector Breakout Signal Trace Routing Issues to Consider

- Voltage withstand minimum spacing required
- Current draw minimum trace width required
- Laminate material used
- Maximum layer count
- Bandwidth needed
- PCB design IPC Class requirement
- Vendor IPC Class capabilities
- Vendor minimum trace/space/trace capability
- Vendor copper plating tolerance
- Remaining space to route traces between finished annular rings under verSI connector
    - See the following for example trace dimension under verSI connector
        - Table 27 - Example IPC Class III, Remaining Space to Route Traces (inch)
        - Figure 70 - Example 100 ohm Edge Coupled Stripline (15mils to Route)
        - Figure 71 - Example 50 ohm Single Ended Stripline (15mils to Route)

Pin Type	PCB Layer	Finished Hole Specification	Finished Hole Tolerance	Finished Hole	+1oz. Plating Thickness	Drill Size	Annular Ring size	Pad Size	Ctr to Ctr of pad	Space to Route Traces
PTH or PIH	External	0.019	0.003	0.019	0.0040	0.0230	0.006	0.0350	0.050	*0.0150*
	Internal	0.019	0.003	0.019	0.0040	0.0230	0.005	0.0330	0.050	*0.0170*
Press fit	External	0.016	0.002	0.016	0.0040	0.0200	0.006	0.0320	0.050	*0.0180*
	Internal	0.016	0.002	0.016	0.0040	0.0200	0.005	0.0300	0.050	*0.0200*

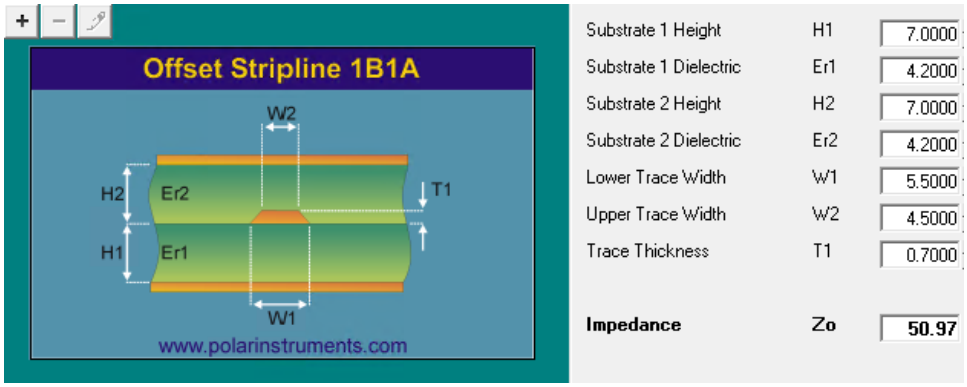
Note: One possible combination. Each PCB vendor may have different recommendations

Table 27 - Example IPC Class III, Remaining Space to Route Traces (inch)



Note: One possible combination. Each PCB vendor may have different recommendations

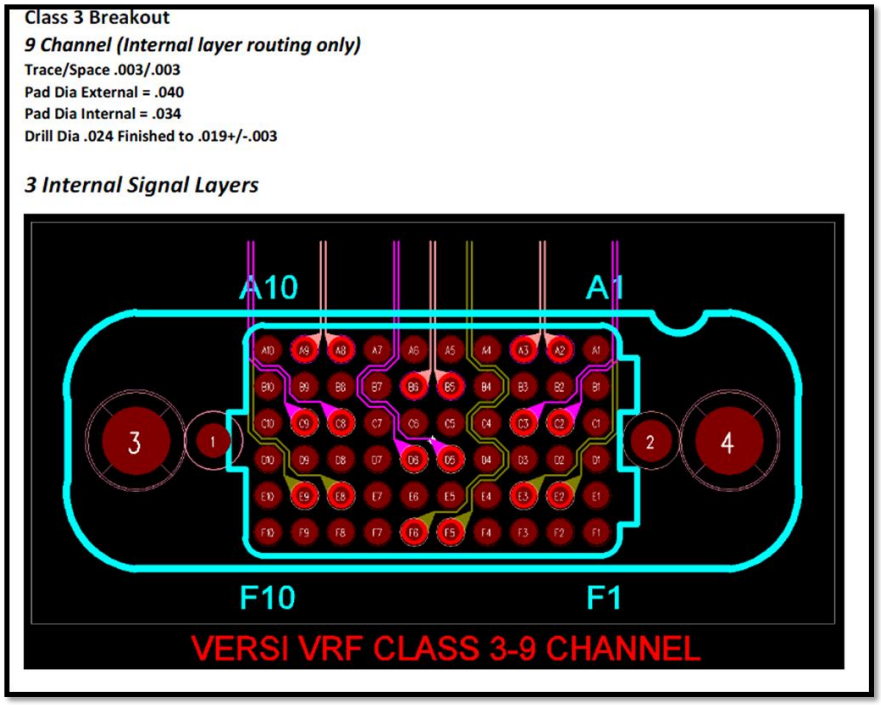
Figure 70 - Example 100 ohm Edge Coupled Stripline (15mils to Route)



Note: One possible combination. Each PCB vendor may have different recommendations

Figure 71 - Example 50 ohm Single Ended Stripline (15mils to Route)

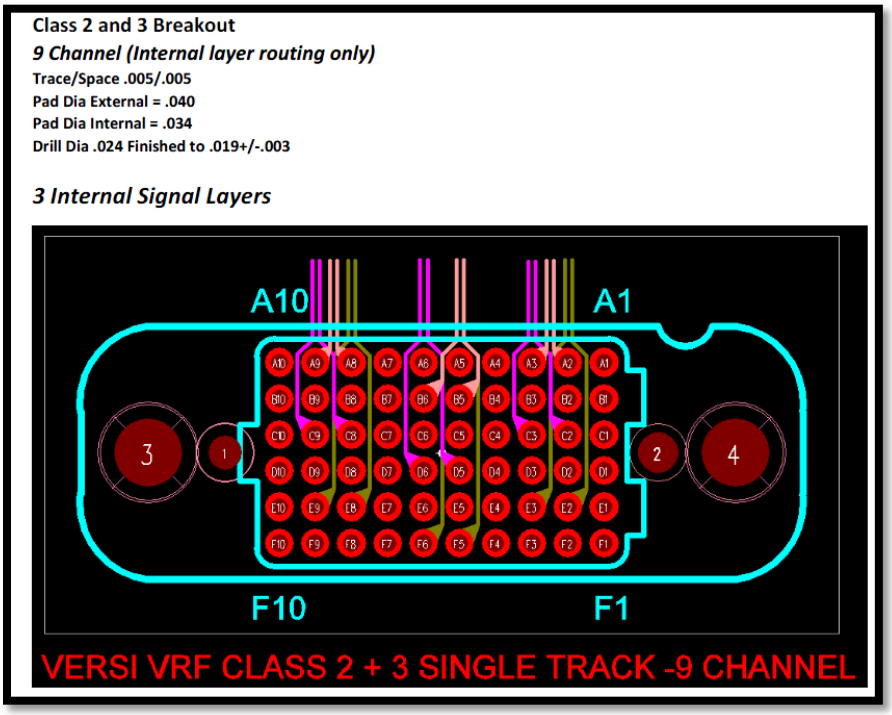
10.7.1 Connector Breakout - “High Speed” Differential Edge Coupled Stripline



Note: Ground planes and anti-pads are not shown

Figure 72 - Example Breakout - High Speed Differential

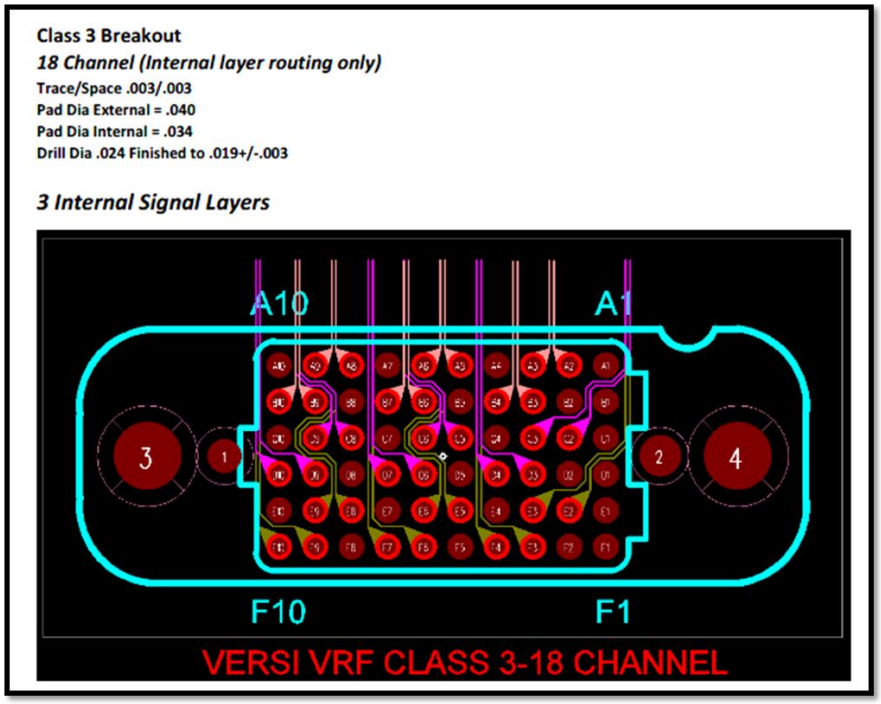
10.7.2 Connector Breakout - “High Speed” Single Ended Stripline



Note: Ground planes and anti-pads are not shown. Some traces route under anti-pads.

Figure 73 - Example Breakout - High Speed Single Ended

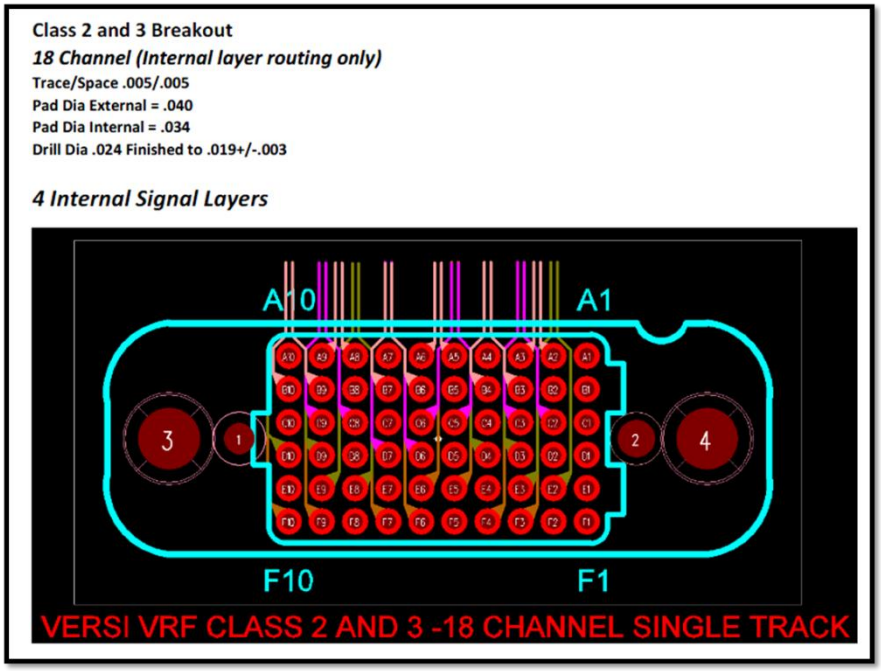
10.7.3 Connector Breakout - “Medium Low Speed” Differential Edge Coupled Stripline



Note: Ground planes and anti-pads are not shown

Figure 74 - Example Breakout - Medium Low Speed Differential

10.7.4 Connector Breakout - “Medium Lower Speed” Single Ended Stripline



Note: Ground planes and anti-pad are not shown. Some traces route under anti-pads.

Figure 75 - Example Breakout - Medium Low Speed Single Ended