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1.0 SCOPE

This report demonstrates the signal integrity performance of the Molex Series 74441 connectors in SFP+ applications. All reported data for connector performance is measurement based. The channel performance data is a hybrid of measured data for the connector and modeled data for the host and module channels.

Disclaimer: Molex does not guarantee the performance of the final product to the information provided in this document. All information in this report is considered Molex proprietary and confidential. This guide is not intended as a substitute for engineering analysis.

2.0 PRODUCT DESCRIPTION

Part number 74441-0001 (20 circuit, 15µ" gold plating)
Part number 74441-0010 (20 circuit, 30µ" gold plating)

3.0 APPLICABLE DOCUMENTS AND SPECIFICATIONS

Product Specification – PS-74441-001
SFP+ Electrical Model – xx-74441-001
SFF-8431 – Specifications for Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable Module "SFP+", Revision 1.1, October 27, 2006

4.0 APPLICATION DESCRIPTION

From SFF-8431:

The SFF-8431 specification defines the electrical interfaces between the host and the SFP+ module for operation up to 11.1 Gbps. The high-speed electrical interface between the host and SFP+ module is called “SFI”. SFI simplifies the module and leverages host based transmit pre-emphasis and host based receive equalization to overcome PCB and fiber impairments.

SFI interface typically operates over 200mm of improved FR41 material or up to about 150 mm of standard FR4 with one connector. The electrical interface is based on high speed low voltage AC coupled logic with a nominal differential impedance of 100 ohms.

The SFP+ module could be an Electrical-to-Optical or an Electrical-to-Electrical multi-rate device, intended to support Datacom applications (10 Gbps Ethernet, 8.5 Gbps Fibre Channel, 10.5 Gbps Fibre Channel, 10 Gb/s Ethernet with FEC) and Telecom (SONET OC-192 and OTU-2). Nominal data rates for these listed standards are given in Table 1 of SFF-8431.

The modules support all data encodings for the above technologies. SFP+ modules common implementations are single mode, multi-mode, or copper electrical-electrical.
5.0 CONNECTOR-ONLY PERFORMANCE

5.1 CONNECTOR TRANSFER, SDD21

Limit of SDD21 (dB) = -0.1 - (0.78 \sqrt{\text{frequency}}) - (0.74 \text{frequency}), \quad 0.25 < \text{frequency (GHz)} < 7

5.2 CONNECTOR TRANSFER RIPPLE

Connector Ripple (dB) = SDD21 (dB) - Linear Fit of SDD21 (dB), \quad \text{Linear fit from 0.25 to 5.5 GHz}

Limits of Ripple (dB) = |0.15 + 0.1 \cdot \text{frequency}|, \quad 0.25 < \text{frequency (GHz)} < 5.5
5.3 CONNECTOR EYE IMPACT

This is a graph showing the impact of the connector only on a transmitted signal. It is based on an 800mv pk-pk, 24ps, 20-80% rise-time, PRBS 9 transmitted signal. The eye mask is the SFI Host Transmitter Output Compliance Mask at B. It demonstrates the significant amount of remaining margin for other channel and system components.

5.4 CONNECTOR IMPEDANCE

The connector impedance as viewed from SFF-8431 compliance points B and C. The rise-time was 24ps (20-80%). The measurement includes a modeled Host Compliance Board that is described in section 7.1 Channel Description of this report.
6.0 SFP+ CHANNEL PERFORMANCE

6.1 CHANNEL DESCRIPTION

The channel is a hybrid model combination of measured s-parameters for the connector and circuit simulation components for the Host and Host Test Boards. The simulation components were parameterized to meet the intentions of SFF-8431.

The connector model was based on measured s-parameters of a Molex Series 74441 20-circuit connector. The effects of the printed circuit board test fixture were removed to within 0.5mm of the interfaces to the connector using on-fixture TRL and LRM calibration structures. The bandwidth of the measured data is from 20 MHz to 20.48GHz using a frequency step of 20MHz (1024 data points). The measurements were taken using an Agilent 8364B 4-port PNA along with Agilent's PLTS software (version 3.120). The s-parameter model as well as further information regarding the measurement fixture and methodology is available upon request. The performance of the connector-only s-parameter model is demonstrated in Section 6, Connector Only Performance, of this report.

The host board model is based on the first entry of common host board designs in Table 2 of SFF-8431. It was realized using Agilent's ADS Libra Microstrip Coupled Lines, MCLIN, component. With 200mm for the trace length (L), 0.3mm for the trace width (W) and 0.2mm for the trace spacing (S). The realized impedance of the modeled host board channel was 100ohms.

<table>
<thead>
<tr>
<th>Type</th>
<th>Material</th>
<th>Trace Width (mm)</th>
<th>Loss Tan</th>
<th>Copper (oz / um)</th>
<th>Trace Length (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Microstrip</td>
<td>4000-6/8</td>
<td>0.3</td>
<td>0.022</td>
<td>1 / 35</td>
</tr>
<tr>
<td></td>
<td>Microstrip</td>
<td>4000-13</td>
<td>0.3</td>
<td>0.016</td>
<td>1 / 35</td>
</tr>
<tr>
<td></td>
<td>Stripline</td>
<td>4000-6/8</td>
<td>0.125</td>
<td>0.022</td>
<td>1 / 35</td>
</tr>
<tr>
<td></td>
<td>Stripline</td>
<td>4000-13</td>
<td>0.125</td>
<td>0.016</td>
<td>1 / 35</td>
</tr>
</tbody>
</table>

SFF-8431, Table 2 - Host Board Configuration

The host compliance test card model is based on Appendix C of SFF-8431. Appendix C recommends the loss from the card resemble to within 15% (see footnote 1, page 49) the reference formula:

\[
SDD21 (\text{dB}) = -0.02 - (0.073 \cdot \sqrt{\text{frequency}}) - (0.088 \cdot \text{frequency}), \quad 0.25 < \text{frequency} (\text{GHz}) < 11
\]
It was also realized using Agilent's ADS Libra Microstrip Coupled Lines, MCLIN, component. With 35mm for the trace length (L), 0.3mm for the trace width (W) and 0.2mm for the trace spacing (S). The model performance versus the reference formula is shown in the following graph. The realized impedance of the model was 100ohms.
6.2 CHANNEL TRANSFER

Max. SDD21 (dB) = -0.1 - (0.78 \cdot \sqrt{\text{frequency}}) - (0.74 \cdot \text{frequency}), 0.25 < \text{frequency} (GHz) < 7

Min. SDD21 (dB) = \frac{1}{3} \cdot (1 - \text{frequency}), 1 < \text{frequency} (GHz) < 7
= -2, 7 < \text{frequency} (GHz) < 11

6.3 CHANNEL TRANSFER RIPPLE

Channel Ripple (dB) = SDD21 (dB) - Linear Fit of SDD21 (dB), Linear fit from 0.25 to 5.5 GHz

Limits of Ripple (dB) = |0.15 + 0.1 \cdot \text{frequency}|, 0.25 < \text{frequency} (GHz) < 5.5
6.4 DIFFERENTIAL RETURN LOSS

This graph represents the return loss of the channel for the Host Receiver Input at C or the Host Transmitter Output at B. The Host System Compliance Test Board was included as instructed in SFF-8431 Sections 3.4.1 and 3.4.2 using the model described earlier. It does not include any return loss information contributed by the ASIC/SerDes and, if included, this signal information would be attenuated by the Host Channel.

SDD11 (dB) = -10  
= -10 + 25 \cdot \log(\text{frequency}/7.5)  
0.01 < \text{frequency} (GHz) < 7.5  
7.5 < \text{frequency} (GHz) < 15
6.5 CHANNEL EYE DIAGRAM

The eye diagram is of a simulated host transmitter differential output at B. It is based on an 800mv pk-pk, 24ps, 20-80% rise-time, PRBS 9 host transmitter launch at channel location A. The eye mask is the SFI Host Transmitter Output Compliance Mask at B. The simulation data meets the eye mask while including the modeled host board, the measured connector s-parameters and the host compliance test board as indicated in SFF-8431 section 3.4.1. The simulation represents the performance of the channel only and does not include any transmitter or receiver generated noise. It does demonstrate the margin left for these noise sources.
6.6 CHANNEL ISOLATION

(Reference Only)

Host NEXT Loss

Module NEXT Loss